

NWQAA

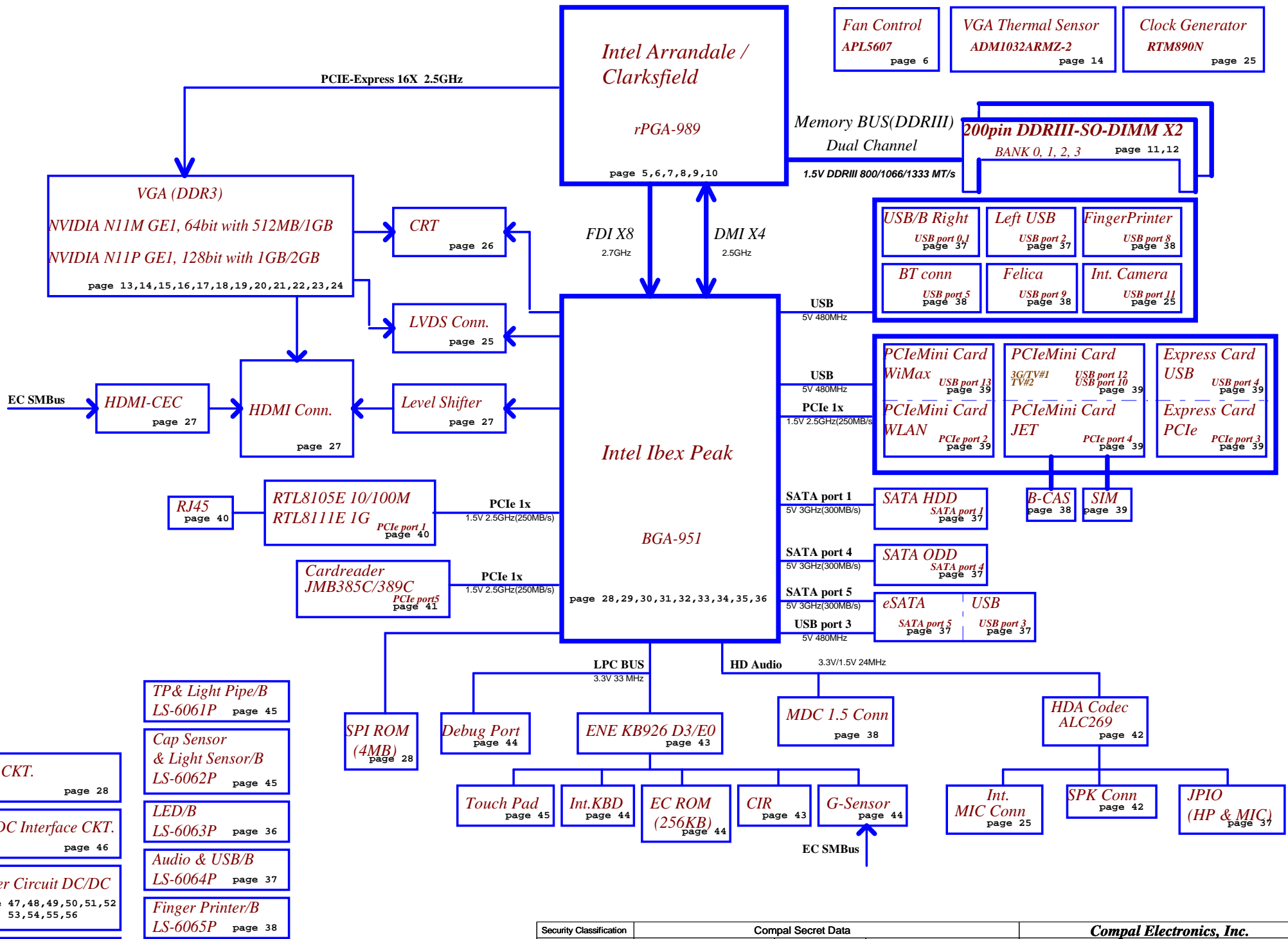
Marseille 10G

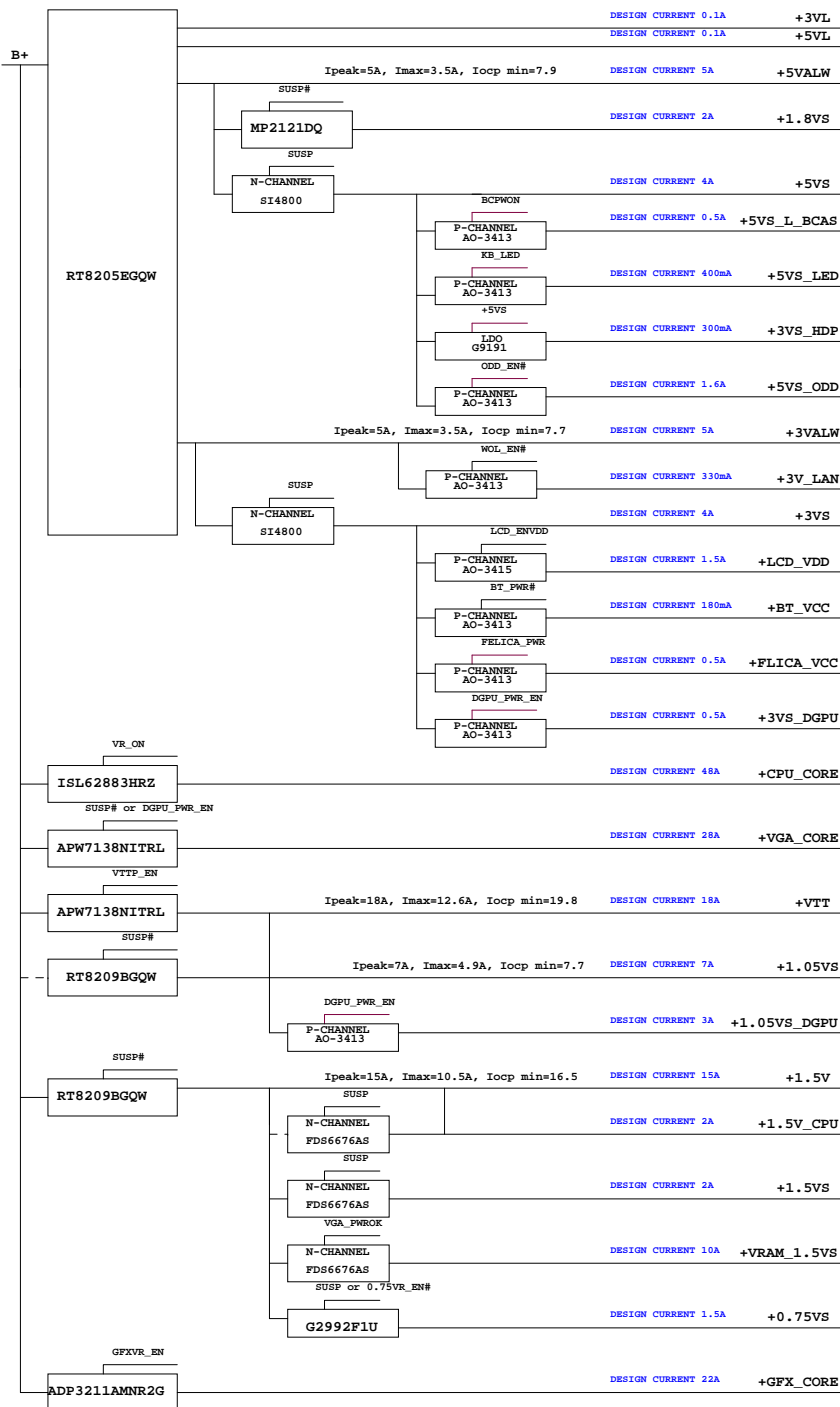
LA-6062P REV 2.0 Schematic

Intel Processor(CFD/ARD) / PCH(HM57/HM55/PM55)

2010-03-24 Rev 2.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Document Number
				Date	Wednesday, March 24, 2010
				Sheet	1 of 59
				Rev	2.0
				Cover Page	
				NWQAA LA-6062P M/B	





Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	Power Tree	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					NWQAA LA-6062P M/B	2.0
				Date	Tuesday, March 23, 2010	Issue 3 of 68

Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1.5VS +3VS_DGPU +1.05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	New Card		
+3VS	WLAN/WIMAX		
+3VS	Clock Generator		
+3VS	3G		

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b	+3VS	PCH	96 H	1001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b	+3VS	NVIDIA GPU	9A H	1001 1010 b
				+3VS	G-Sensor	40 H	0100 0000 b
				+3VS	Light Sensor	52 H	0101 0010 b
Power	Device	HEX	Address				
+3VL	Cap. Sensor		Virtual I2C				

Platform	SKU	CPU	PCH	VGA
Calpella	UMA(OPT@)	Arrandale	HM55@/HM57@	N/A
	Discrete (DIS@)	Clarksfield/Arrandale	HM55@/HM57@/PM55@	N11P@/N11M@
	Optimus (OPT@)	Arrandale	HM55@/HM57@	N11P@/N11M@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	Modem	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	Modem	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	Modem	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	MDC@	CIR@	KBL@

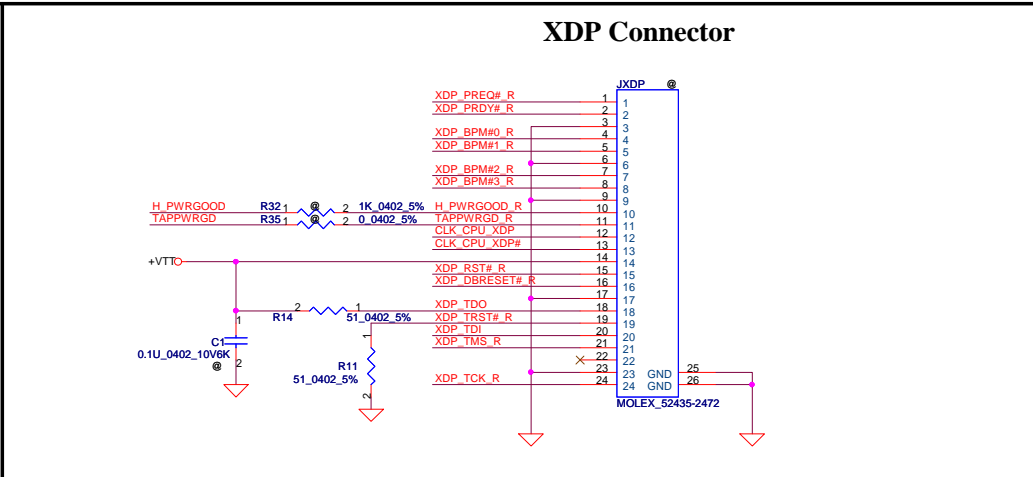
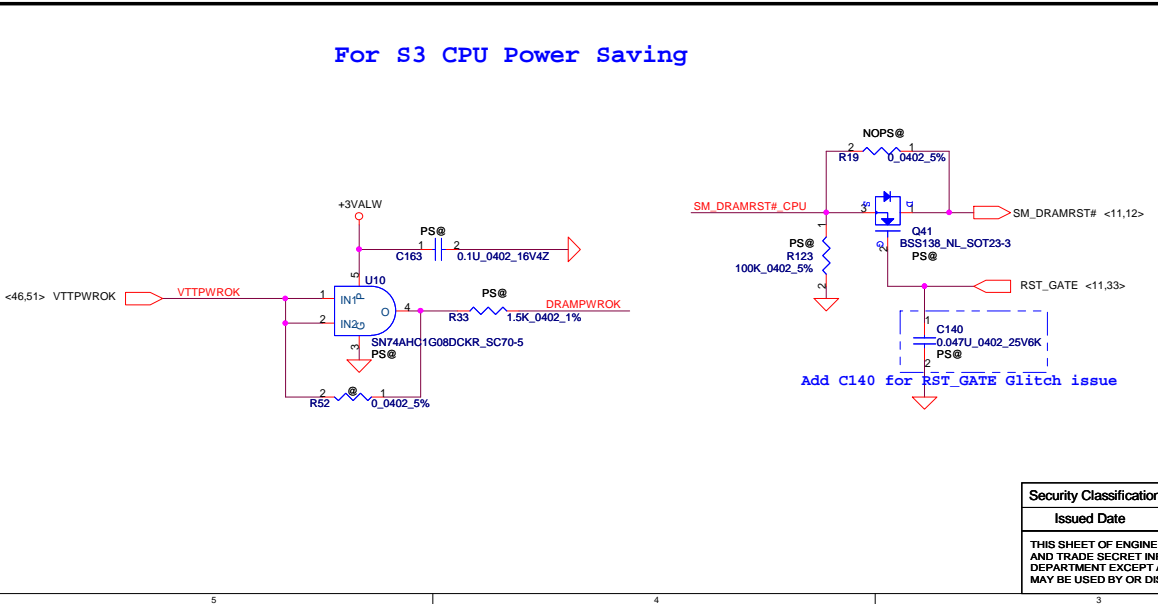
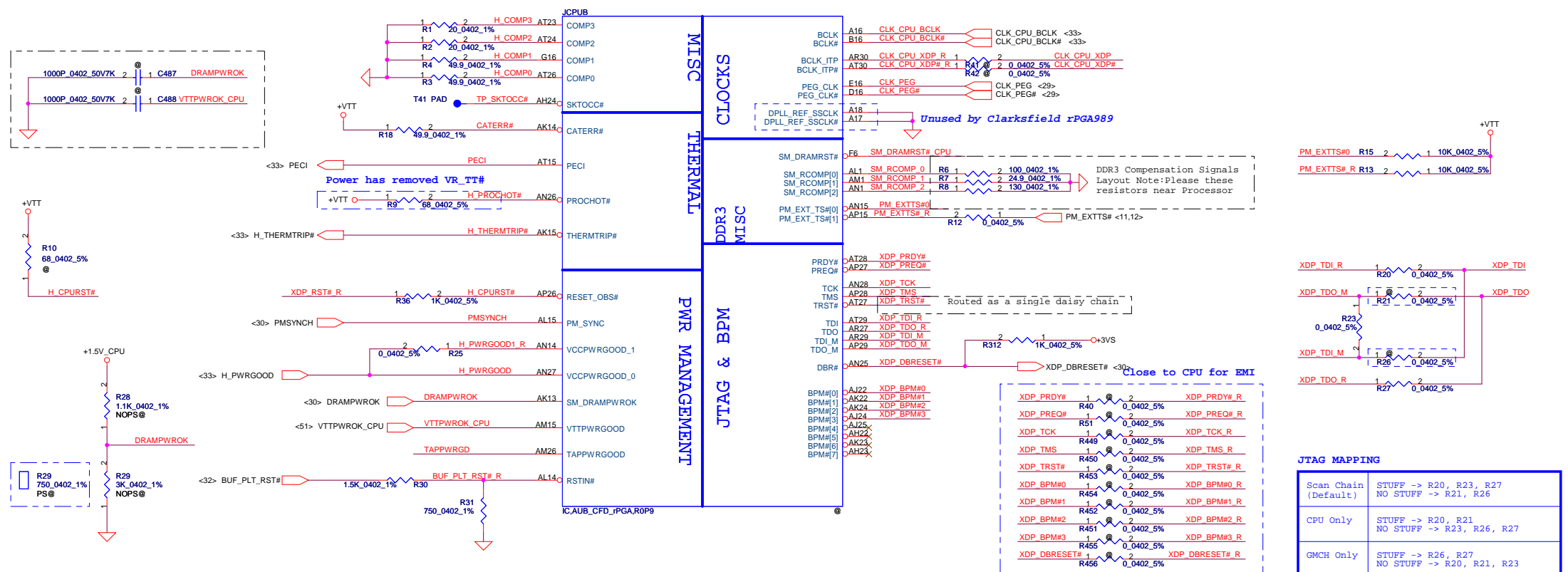
Function	Felica	BLUE TOOTH	G-SENSOR	SKU		LVDS		Camera & Mic	
description	Felica	BLUE TOOTH	G-SENSOR	SKU		3D Panel		Camera & Mic	
explain	Felica	BLUE TOOTH	G-SENSOR	Discrete	Optimus	Discrete		Optimus	Camera & Mic
BTO	FELICA@	BT@	GSSENSOR@	DIS@	OPT@	3D@	NO3D@	OPTFH@	CAM@

Function	S3 Power Saving		GPU					New Card
description	S3 Power Saving		N11P & N11E			N11M		New Card
explain	No Power Saving	Power Saving	VRAM	N11P	N11E	N11M-GE1	N11M-OP1	New Card
BTO	NOPS@	PS@	8PCS@	N11P@	N11E@	N11MGE@	N11MOP@	NEW@

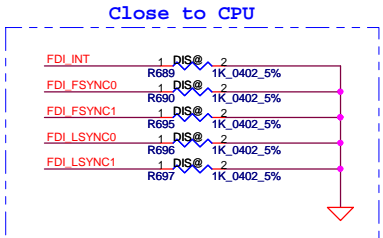
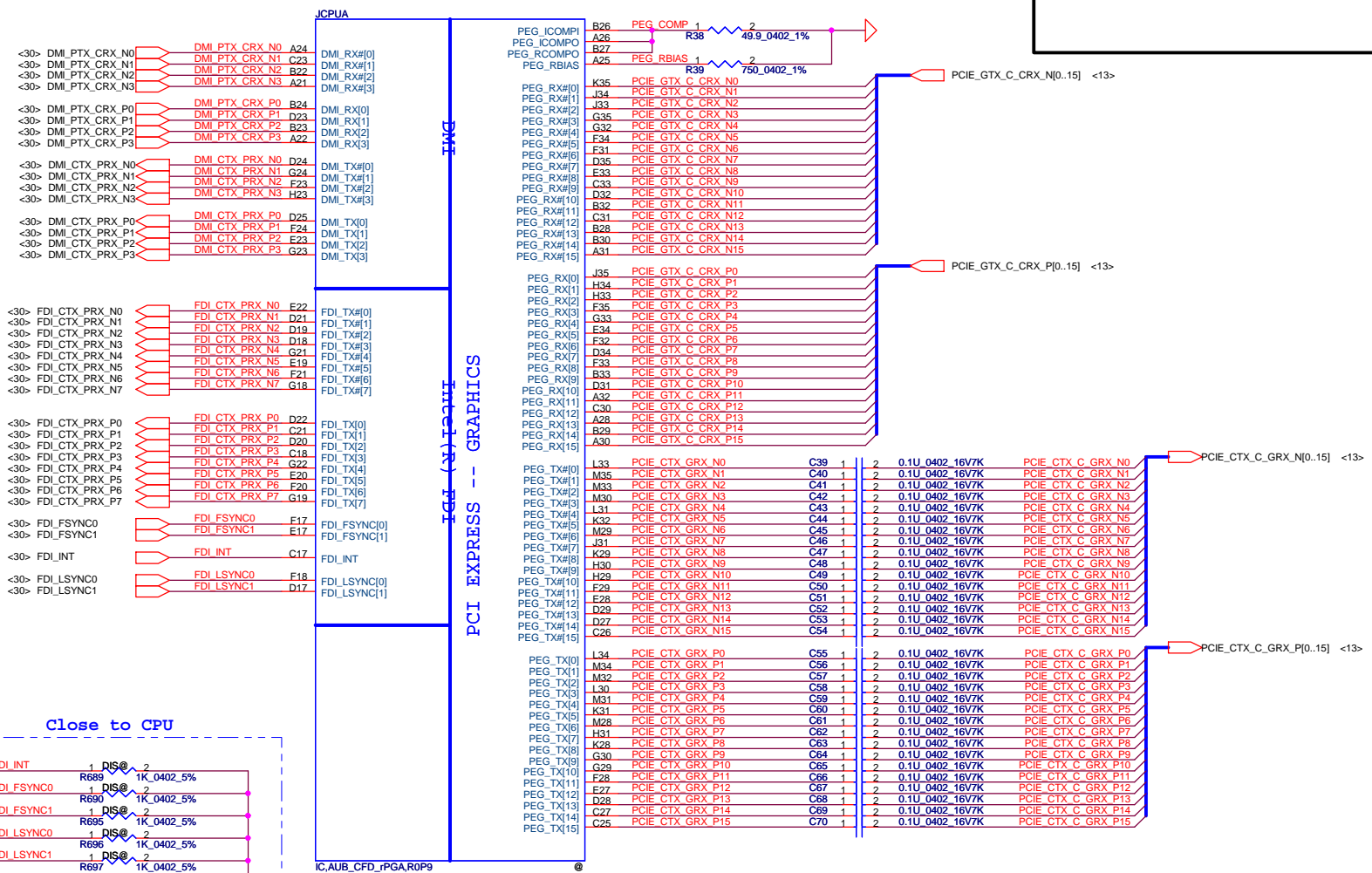
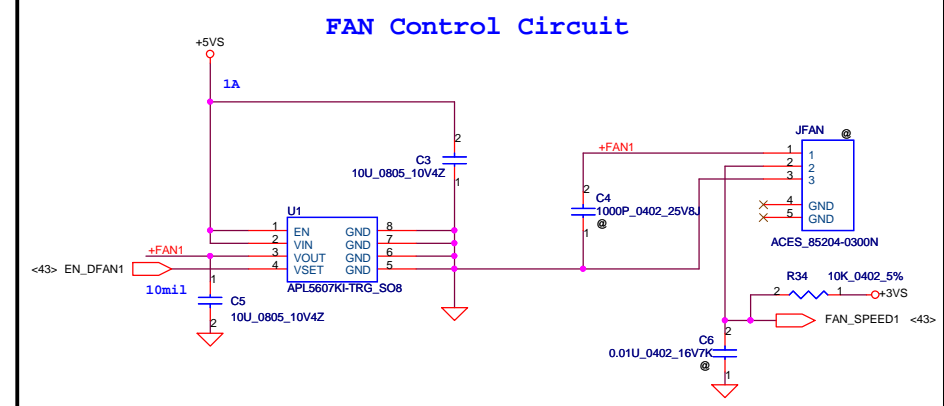
Function	Card reader	
description	JMB385C/389C	
explain	JMB385C	JMB389C
BTO	JMB385@	JMB389@

STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

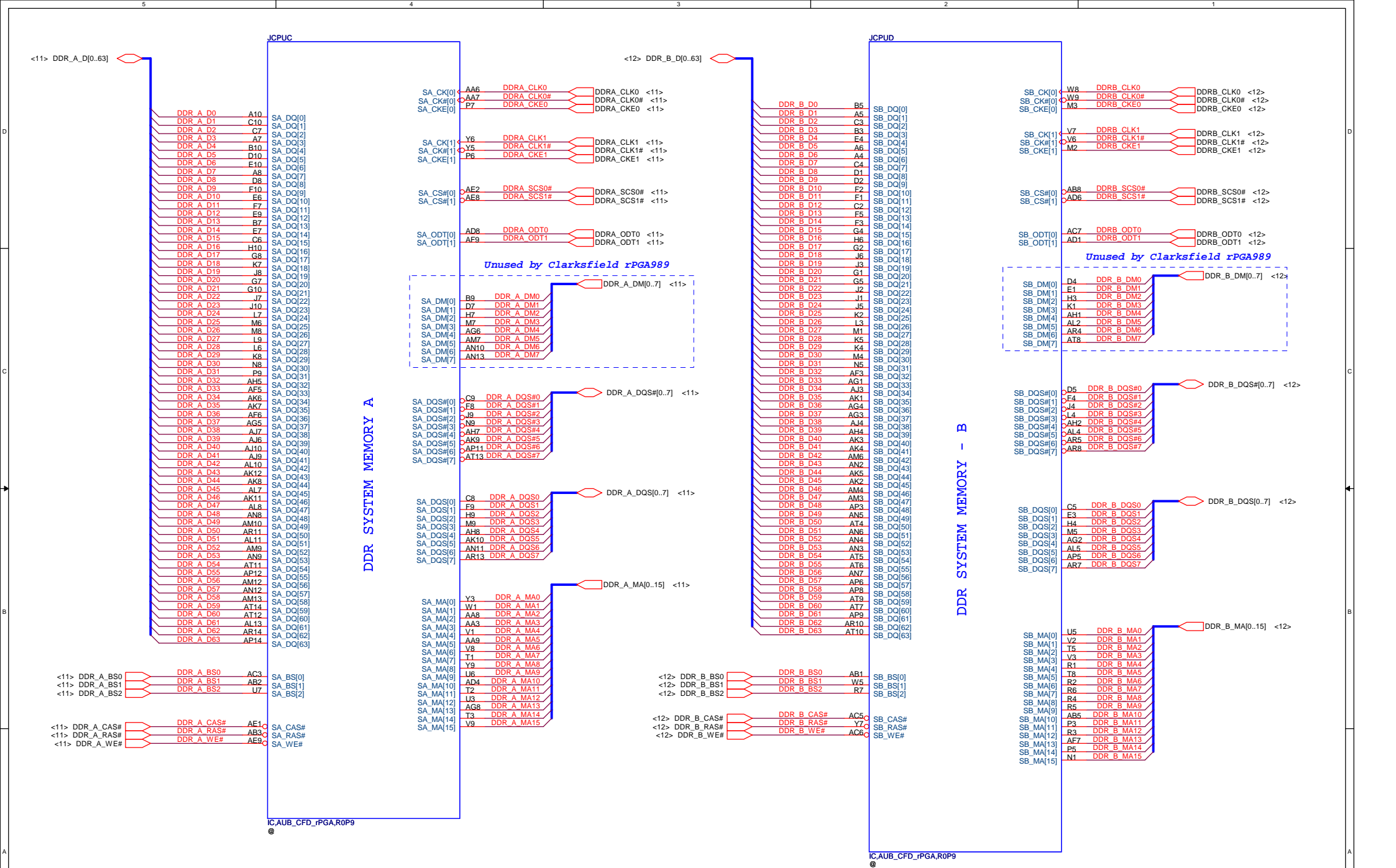
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	200910/9	Deciphered Date	2010/01/23	Notes List		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number	Rev 2.0
				Date:	Tuesday, March 23, 2010	Sheet 4 of 59



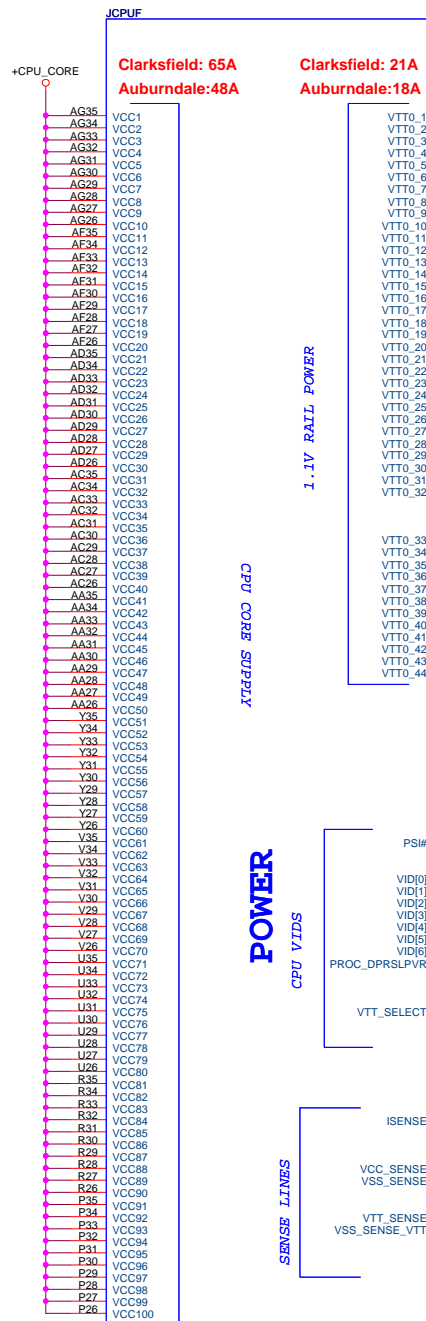
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	CPU_CLK/MISC/JTAG/XDP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Custom
				Document Number	NWQAA LA-6062P M/B
				Rev	2.0
				Date	Wednesday, March 24, 2010
				Sheet	5 of 59



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	CPU_DMI/FDI/PEG/FAN	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				NWQAA LA-6062P M/B	2.0
				Date	Wednesday, March 24, 2010
				Sheet	6 of 59



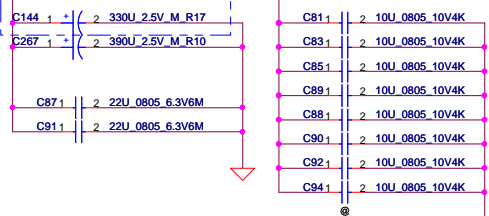
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size B	Document Number
				Rev 2.0	
				Date:	Wednesday, March 24, 2010
				Sheet	7 of 59



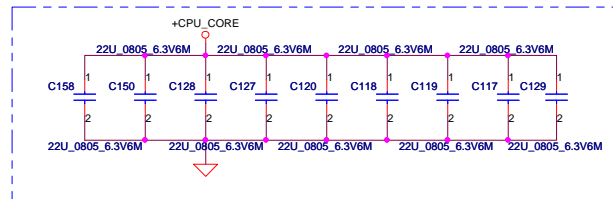
Material Note (+VTT):
390uF/ 10mohm, number are 3,
power x1, HW x2

(Place these capacitors under CPU socket Edge, top layer)

Change C144 to 4.5mm height at DVT



5/25: Add for power team request.

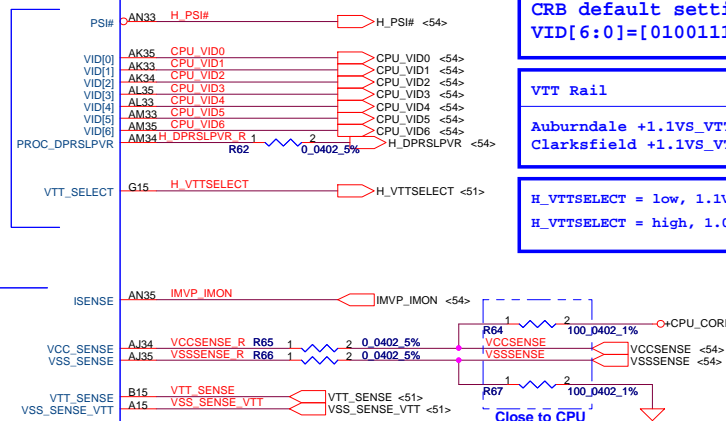


CRB default setting:
VID[6:0]=[0100111]

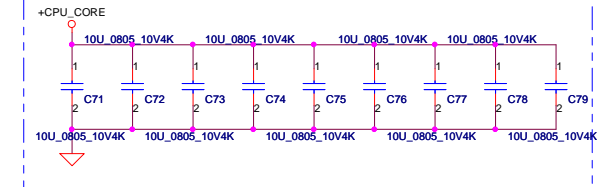
VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

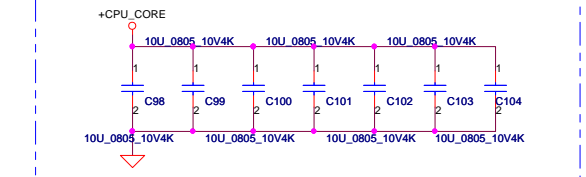
H_VTTSELECT = low, 1.1V
H_VTTSELECT = high, 1.05V



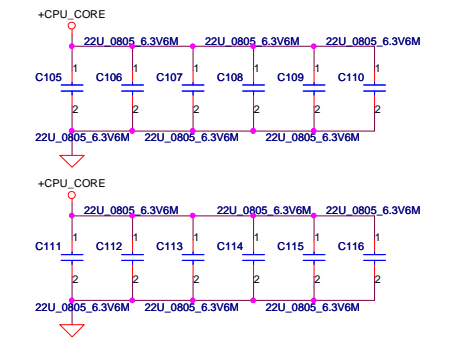
(Place these capacitors between inductor and socket on Bottom)



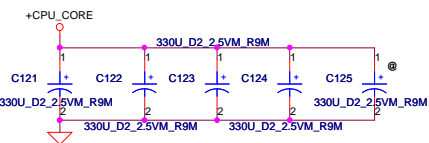
(Place these capacitors under CPU socket, top layer)



(Place these capacitors on CPU cavity, Bottom Layer)



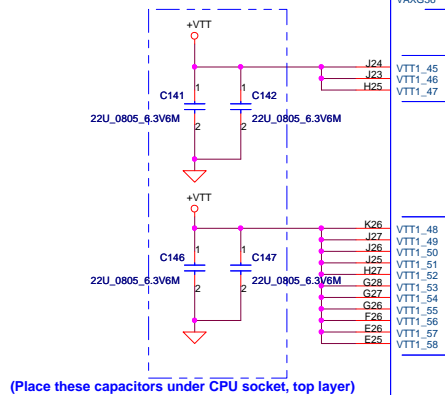
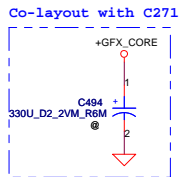
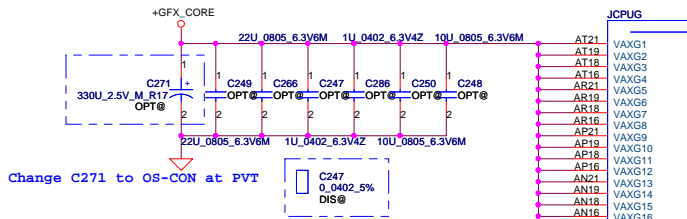
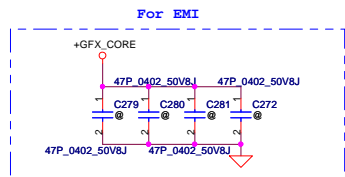
TOP side (under inductor)



Check list:

+CPU_CORE: 6x 470uF, 12x 22uF, 17x 10uF
+VTT: 4x 330uF, 7x 22uF, 8x 10uF

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/10/9	Deciphered Date	2010/01/23	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				Rev
				2.0
				Date: Wednesday, March 24, 2010
				Sheet 8 of 59



22A
GRAPHICS

POWER
FDI

PEG & DMI

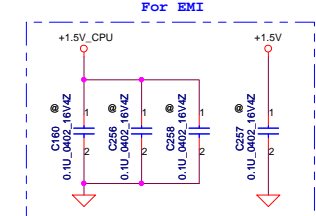
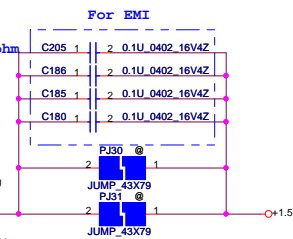
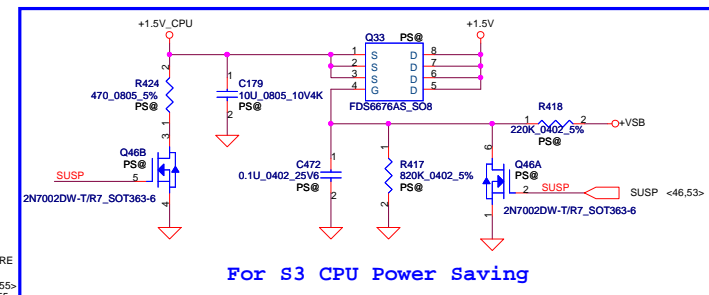
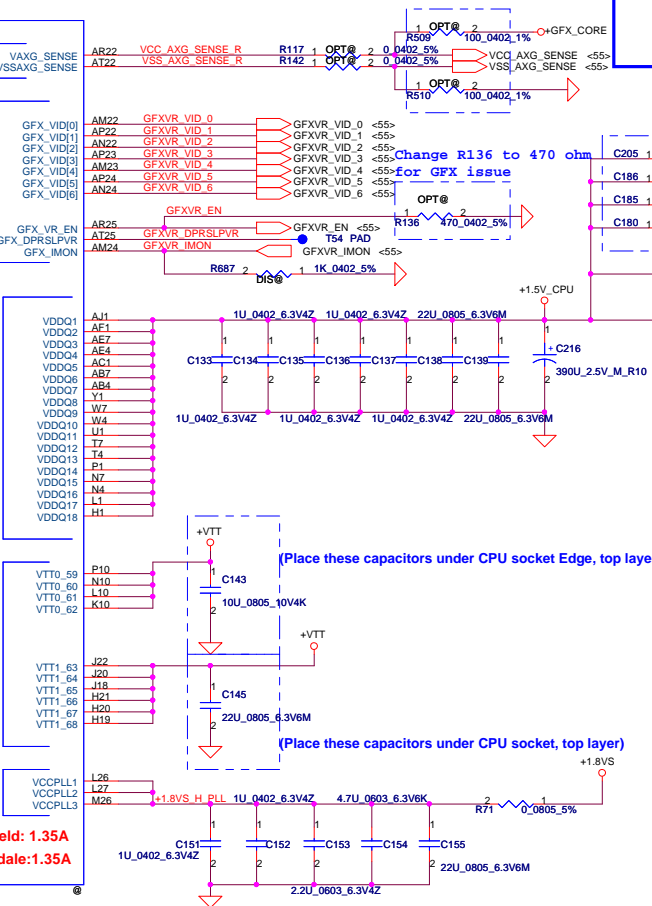
Clarksfield: 1.35A
Auburndale: 1.35A

SENSE LINES

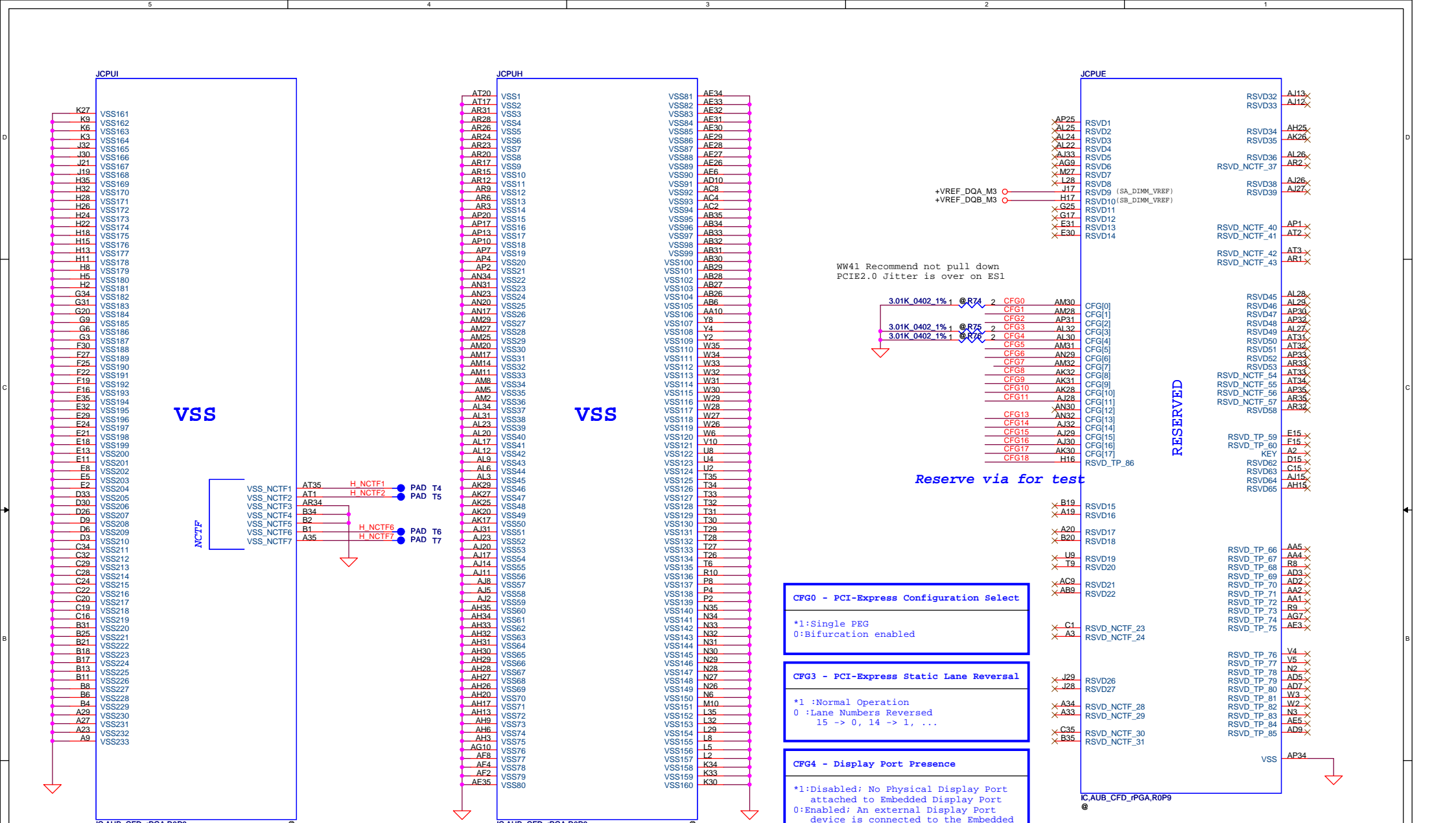
GRAPHICS VIDS

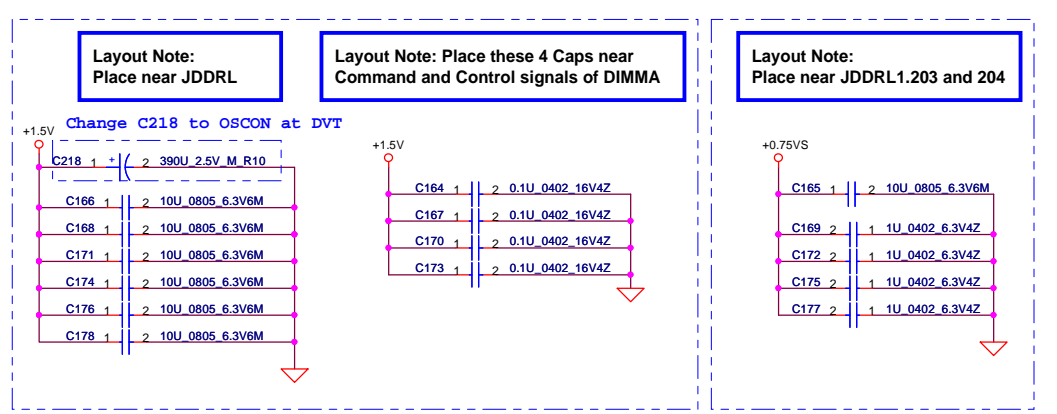
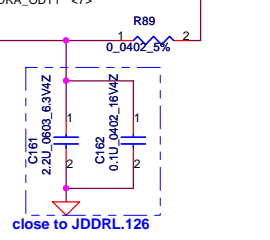
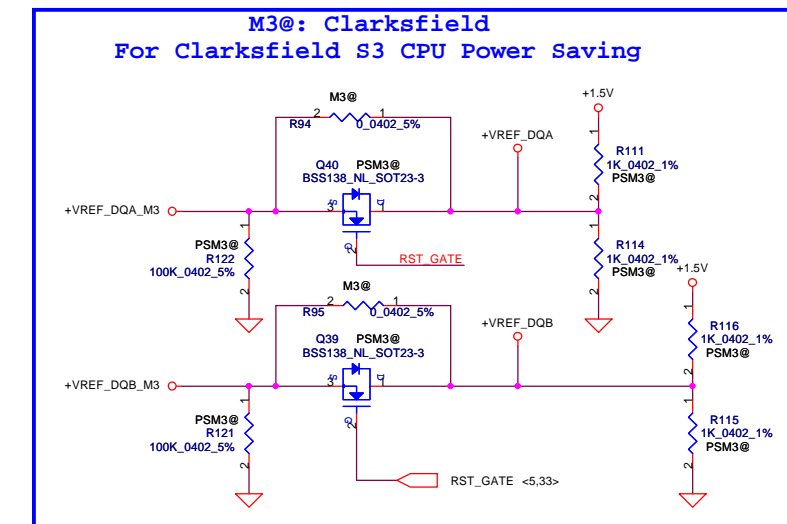
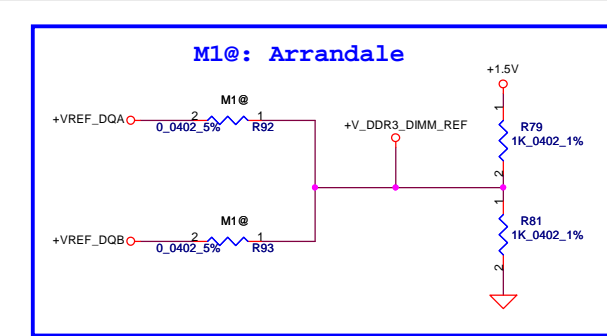
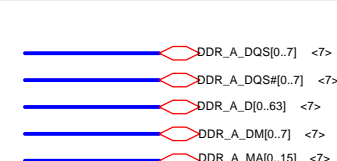
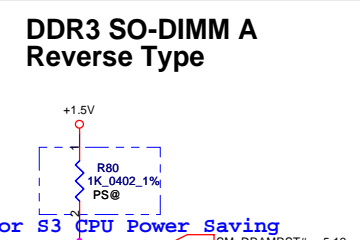
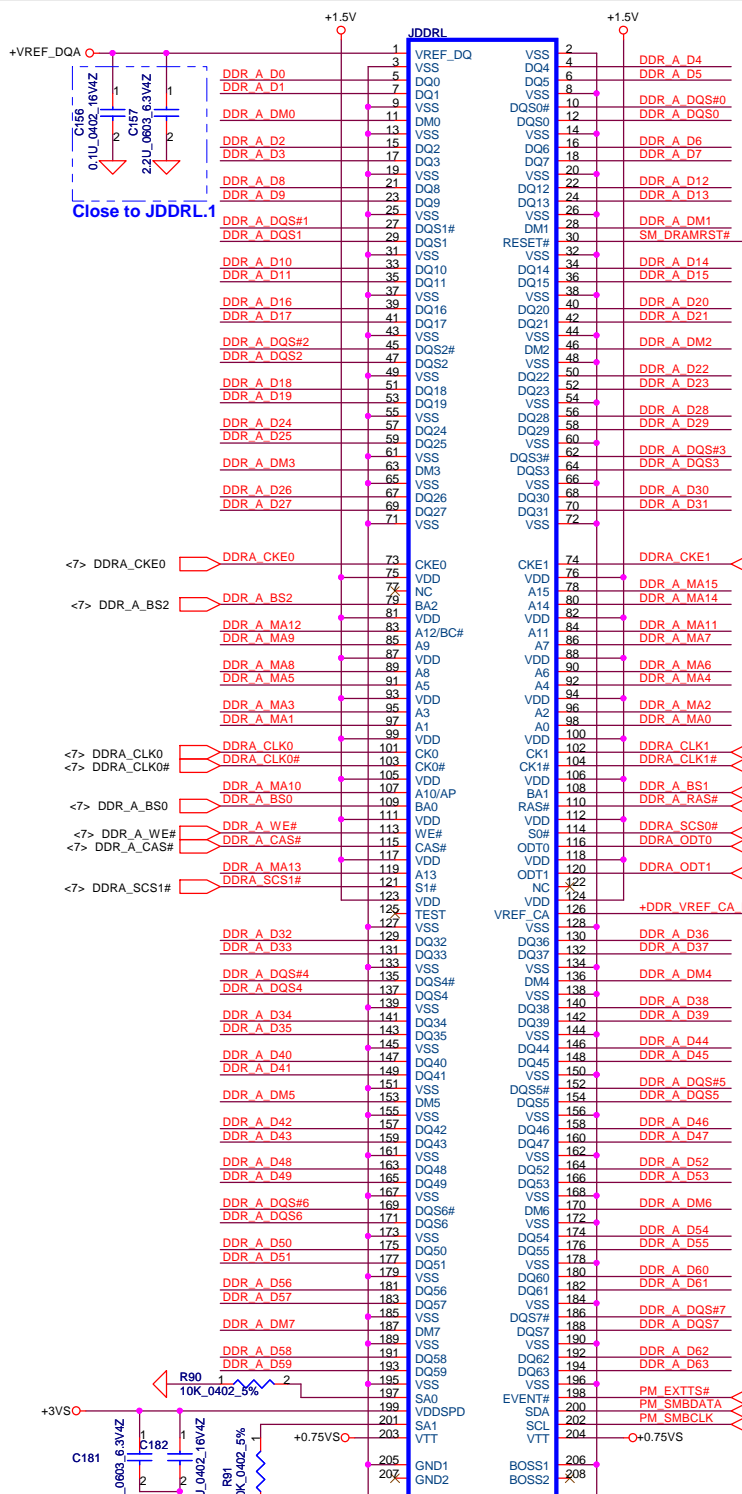
DDR3 - 1.5V RAILS

1.1V
1.8V

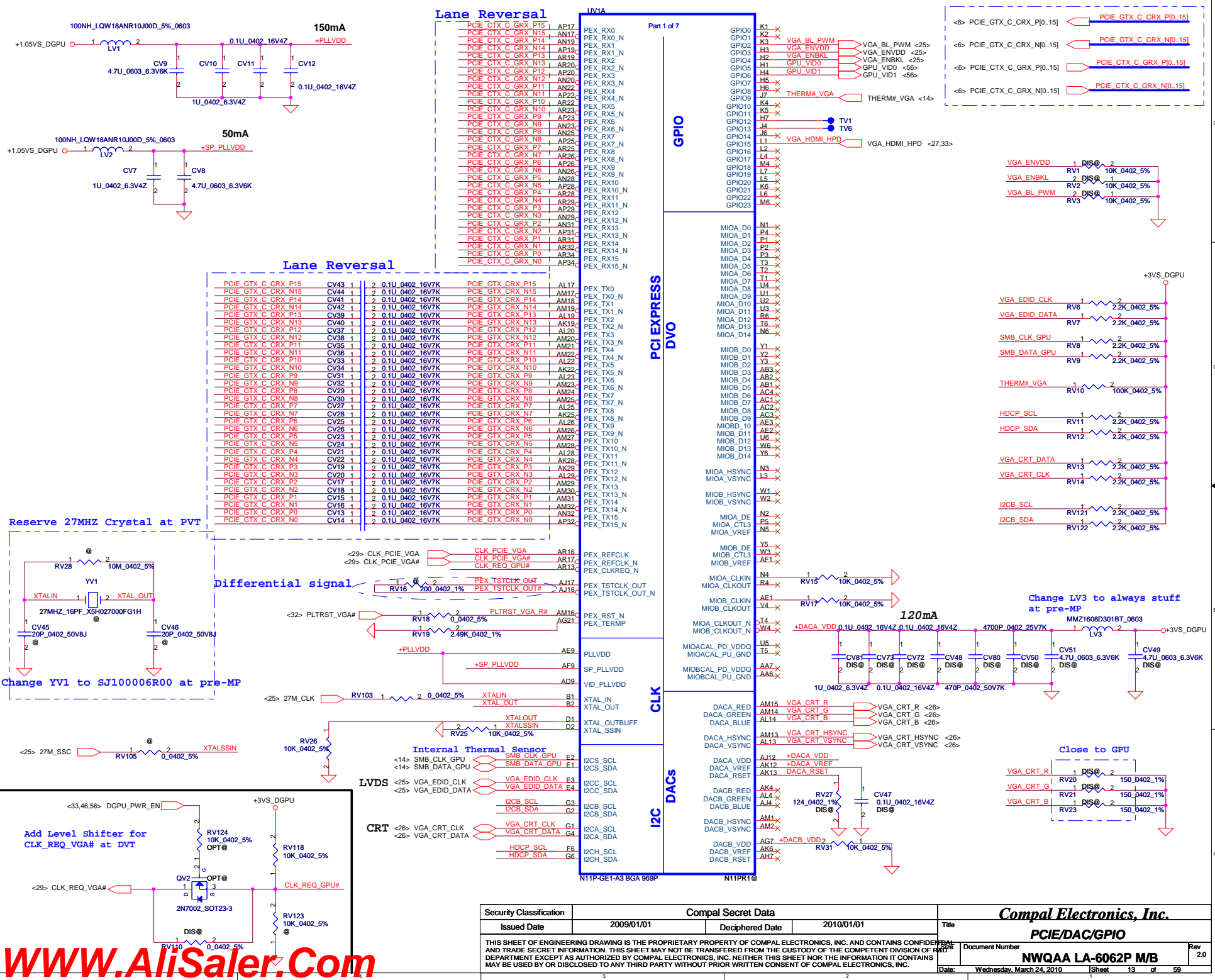


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom
				Document Number NWQAA LA-6062P M/B
				Rev 2.0
				Date: Wednesday, March 24, 2010
				Sheet 9 of 59

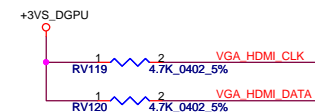
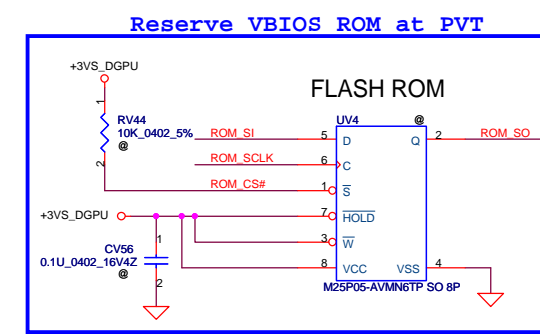
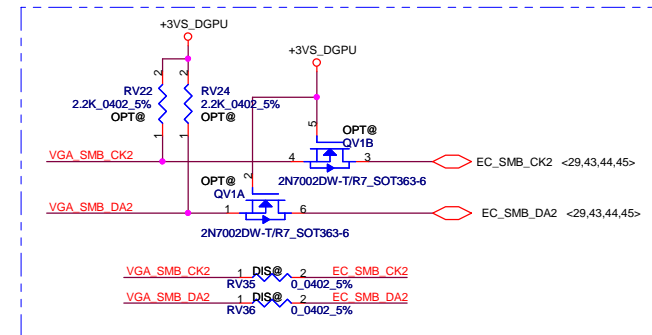
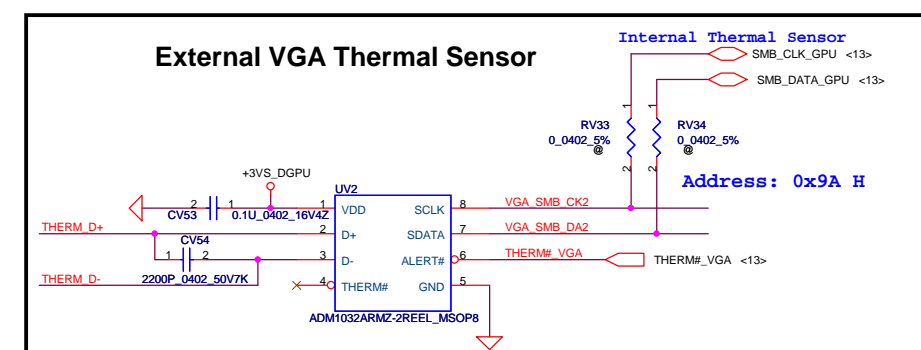
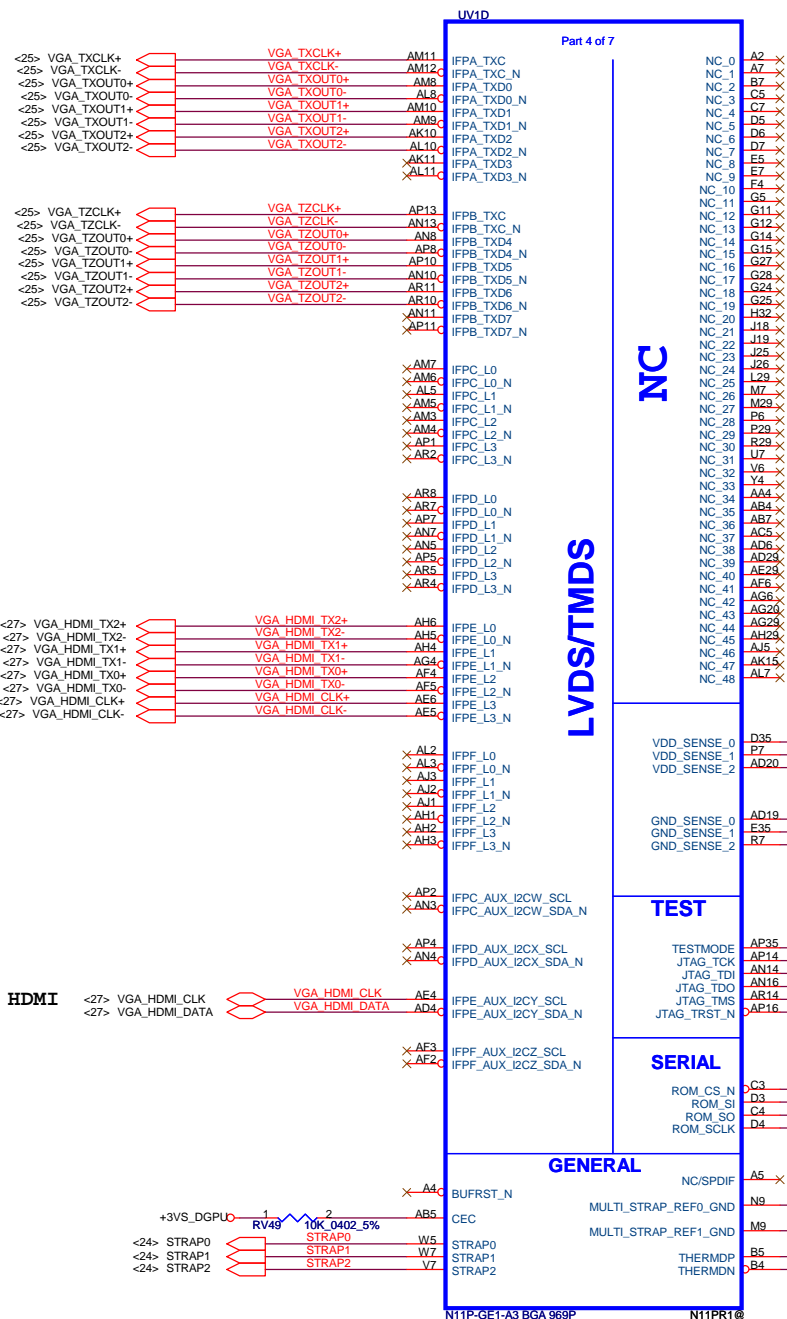




Security Classification				Compal Secret Data				Compal Electronics, Inc.		
Issued Date		200910/9		Deciphered Date		2010/01/23		Title		
								DDRIII-SODIMMO		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								Size	Document Number	Rev
								Custom	NWQAA LA-6062P M/B	2.0
								Date:	Wednesday, March 24, 2010	Sheet 11 of 59



Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	PCIE/DAC/GPIO	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. ANY TRADE SECRET INFORMATION TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				NWQAA LA-6062P M/B	2.0
				Date: Wednesday, March 24, 2010	Sheet 13 of 59



Security Classification	Compal Secret Data			Title	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	Rev	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				NWQAA LA-6062P M/B	2.0
				Date	Sheet
				Wednesday, March 24, 2010	14 of 59

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	450	790	0.90 V
P8	405	324	0.85 V
P12	135	135	0.80 V

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	575	790	0.95 V
P8	405	324	0.85 V
P12	135	135	0.80 V

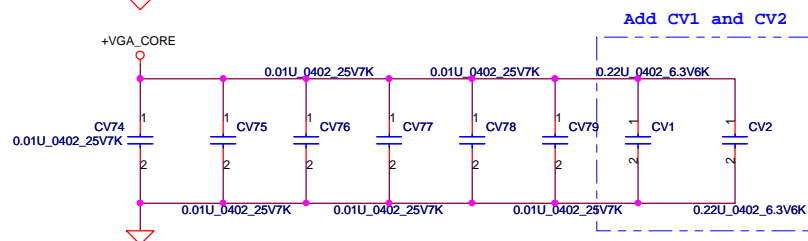
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	625	790	1.03 V
P8	405	405	0.85 V
P12	135	135	0.85 V



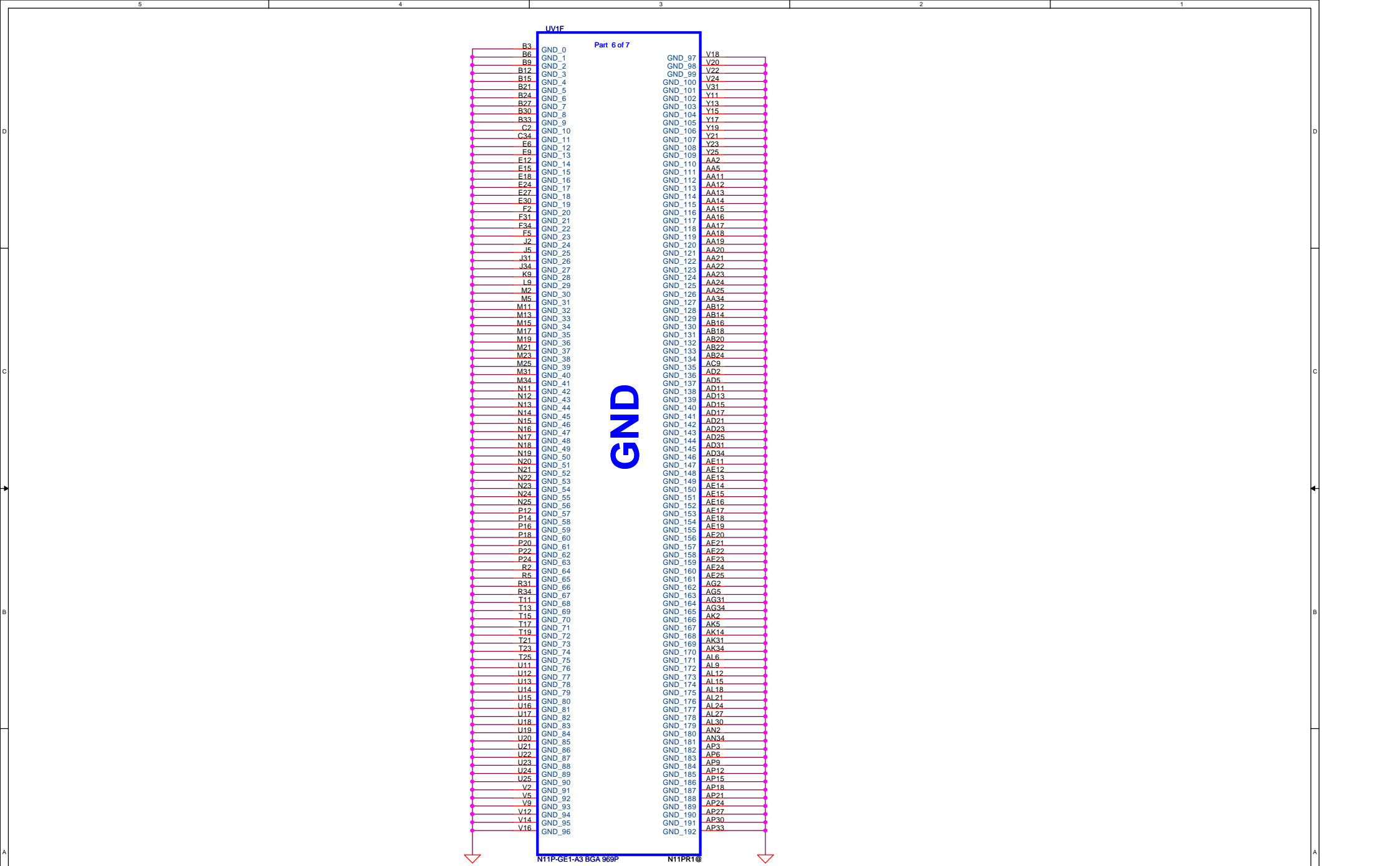
[-OP1 **+VGA CORE** **Change CV57 and CV58 to OS-CON at PVT**

CV57 + CV58

330U_2.5V_M_R17 330U_2.5V_M_R17



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	Title	VGA CORE
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No	Rev
				Document Number	2.0
				Date:	Tuesday, March 23, 2010
				Sheet	15 of 59



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	Title	GND
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Date	Tuesday, March 23, 2010
				Sheet	17 of 59
				Rev	2.0
				NWQAA LA-6062P M/B	

<20,21> MDA[0..63] MDA[0..63]

UV1B

Part 2 of 7

MDA0	L32	FBA_D0
MDA1	N33	FBA_D1
MDA2	L33	FBA_D2
MDA3	N34	FBA_D3
MDA4	N35	FBA_D4
MDA5	P35	FBA_D5
MDA6	P33	FBA_D6
MDA7	P34	FBA_D7
MDA8	K35	FBA_D8
MDA9	K33	FBA_D9
MDA10	K34	FBA_D10
MDA11	H33	FBA_D11
MDA12	G34	FBA_D12
MDA13	G33	FBA_D13
MDA14	E34	FBA_D14
MDA15	E33	FBA_D15
MDA16	G31	FBA_D16
MDA17	F30	FBA_D17
MDA18	G30	FBA_D18
MDA19	G32	FBA_D19
MDA20	K30	FBA_D20
MDA21	K32	FBA_D21
MDA22	H30	FBA_D22
MDA23	K31	FBA_D23
MDA24	L31	FBA_D24
MDA25	L30	FBA_D25
MDA26	M32	FBA_D26
MDA27	N30	FBA_D27
MDA28	M30	FBA_D28
MDA29	P31	FBA_D29
MDA30	R32	FBA_D30
MDA31	R30	FBA_D31
MDA32	AG30	FBA_D32
MDA33	AG32	FBA_D33
MDA34	AH31	FBA_D34
MDA35	AF31	FBA_D35
MDA36	AF30	FBA_D36
MDA37	AE30	FBA_D37
MDA38	AC32	FBA_D38
MDA39	AD30	FBA_D39
MDA40	AN33	FBA_D40
MDA41	AL31	FBA_D41
MDA42	AM33	FBA_D42
MDA43	AK30	FBA_D43
MDA44	AK32	FBA_D44
MDA45	AJ30	FBA_D45
MDA46	AH30	FBA_D46
MDA47	AH33	FBA_D47
MDA48	AH33	FBA_D48
MDA49	AH35	FBA_D49
MDA50	AH34	FBA_D50
MDA51	AH32	FBA_D51
MDA52	AJ33	FBA_D52
MDA53	AL35	FBA_D53
MDA54	AM34	FBA_D54
MDA55	AM35	FBA_D55
MDA56	AF33	FBA_D56
MDA57	AE32	FBA_D57
MDA58	AE35	FBA_D58
MDA59	AE34	FBA_D59
MDA60	AE34	FBA_D60
MDA61	AE33	FBA_D61
MDA62	AB32	FBA_D62
MDA63	AC35	FBA_D63

MEMORY INTERFACE
A

FBA_CMD0	V32	CMDA0	CMDA0 <20>
FBA_CMD1	W31	CMDA1	CMDA1 <20,21>
FBA_CMD2	U31	CMDA2	CMDA2 <20>
FBA_CMD3	Y32	CMDA3	CMDA3 <20,21>
FBA_CMD4	AB35	CMDA4	CMDA4 <20,21>
FBA_CMD5	AB34	CMDA5	CMDA5 <20,21>
FBA_CMD6	W35	CMDA6	CMDA6 <20,21>
FBA_CMD7	W33	CMDA7	CMDA7 <20,21>
FBA_CMD8	W30	CMDA8	CMDA8 <20,21>
FBA_CMD9	T34	CMDA9	CMDA9 <20,21>
FBA_CMD10	T35	CMDA10	CMDA10 <20,21>
FBA_CMD11	AB31	CMDA11	CMDA11 <21>
FBA_CMD12	Y30	CMDA12	CMDA12 <20,21>
FBA_CMD13	Y34	CMDA13	CMDA13 <20,21>
FBA_CMD14	W32	CMDA14	CMDA14 <20,21>
FBA_CMD15	AA30	CMDA15	CMDA15 <20,21>
FBA_CMD16	AA32	CMDA16	CMDA16 <21>
FBA_CMD17	Y33	CMDA17	CMDA17 <20,21>
FBA_CMD18	U32	CMDA18	CMDA18 <20,21>
FBA_CMD19	Y31	CMDA19	CMDA19 <20,21>
FBA_CMD20	U34	CMDA20	CMDA20 <20,21>
FBA_CMD21	Y35	CMDA21	CMDA21 <20,21>
FBA_CMD22	W34	CMDA22	CMDA22 <20,21>
FBA_CMD23	V30	CMDA23	CMDA23 <20,21>
FBA_CMD24	U35	CMDA24	CMDA24 <20,21>
FBA_CMD25	U30	CMDA25	CMDA25 <20>
FBA_CMD26	U33	CMDA26	CMDA26 <20,21>
FBA_CMD27	AB30	CMDA27	CMDA27 <21>
FBA_CMD28	AB33	CMDA28	CMDA28 <20,21>
FBA_CMD29	T33	CMDA29	CMDA29 <20,21>
FBA_CMD30	W29	CMDA30	CMDA30 <20,21>

FBA_DQM0	P32	DQMA0	DQMA[7..0] <20,21>
FBA_DQM1	H34	DQMA1	
FBA_DQM2	J30	DQMA2	
FBA_DQM3	P30	DQMA3	
FBA_DQM4	AF32	DQMA4	
FBA_DQM5	AL32	DQMA5	
FBA_DQM6	AL34	DQMA6	
FBA_DQM7	AF35	DQMA7	

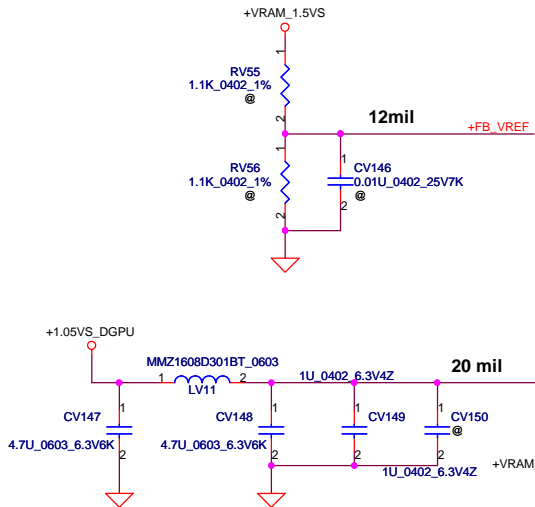
FBA_DQS_RN0	L35	DQSA#0	DQSA#[7..0] <20,21>
FBA_DQS_RN1	G35	DQSA#1	
FBA_DQS_RN2	H31	DQSA#2	
FBA_DQS_RN3	N32	DQSA#3	
FBA_DQS_RN4	AD32	DQSA#4	
FBA_DQS_RN5	AJ31	DQSA#5	
FBA_DQS_RN6	AJ35	DQSA#6	
FBA_DQS_RN7	AC34	DQSA#7	

FBA_DQS_WP0	L34	DQSA0	DQSA[7..0] <20,21>
FBA_DQS_WP1	H35	DQSA1	
FBA_DQS_WP2	J32	DQSA2	
FBA_DQS_WP3	N31	DQSA3	
FBA_DQS_WP4	AE31	DQSA4	
FBA_DQS_WP5	AJ32	DQSA5	
FBA_DQS_WP6	AJ34	DQSA6	
FBA_DQS_WP7	AC33	DQSA7	

FBA_CLK0	T32	CLKA0	CLKA0 <20>
FBA_CLK0_N	T31	CLKA0#	CLKA0# <20>
FBA_CLK1	AC31	CLKA1	CLKA1 <21>
FBA_CLK1_N	AC30	CLKA1#	CLKA1# <21>

Mode C - Mirror Mode Mapping

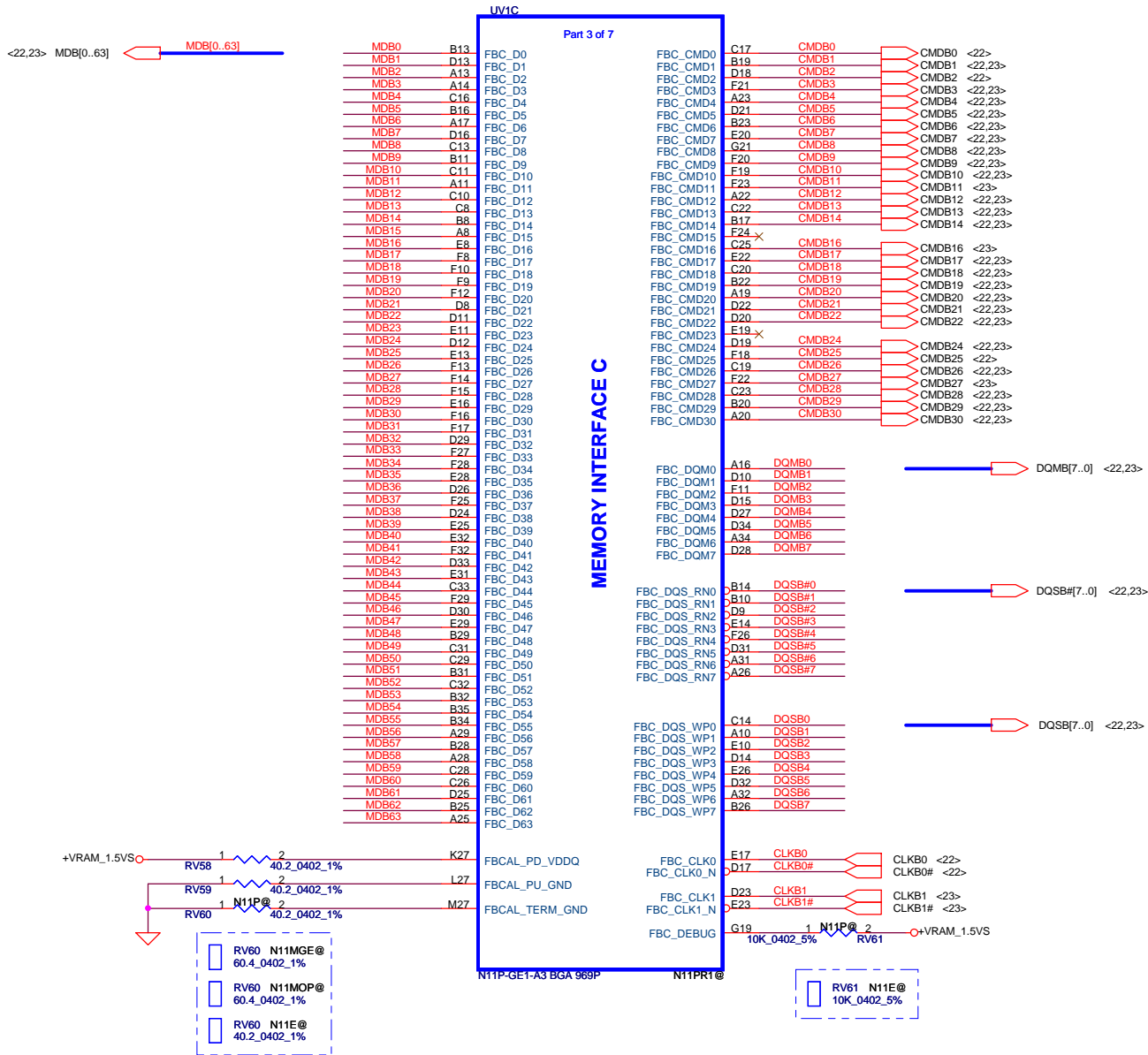
Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2



N11P-GE1-A3 BGA 969P

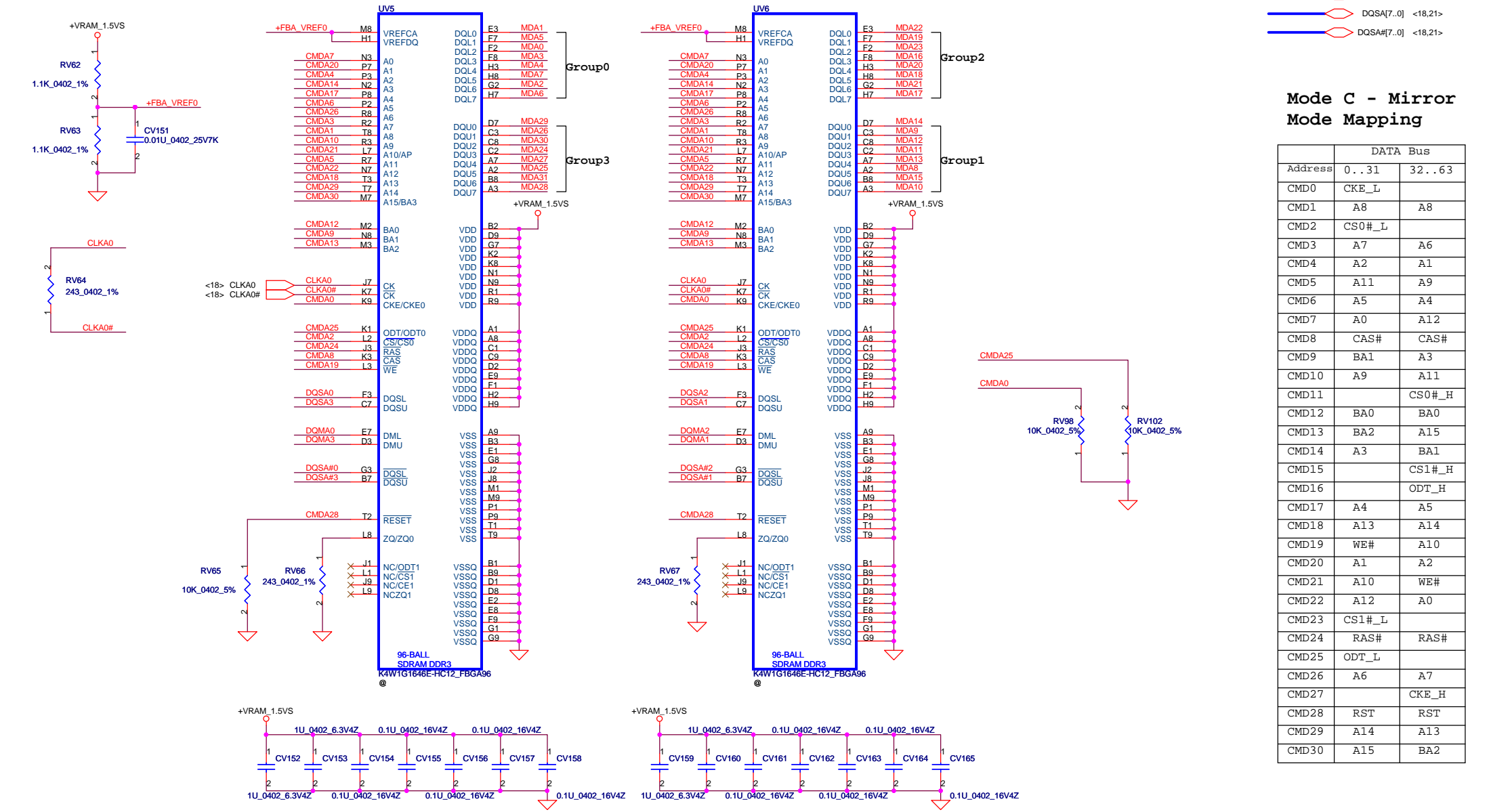
N11PR1@

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	MEM Interface A	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 2.0
				NWQAA LA-6062P M/B	
				Date: Wednesday, March 24, 2010	Sheet 18 of 59

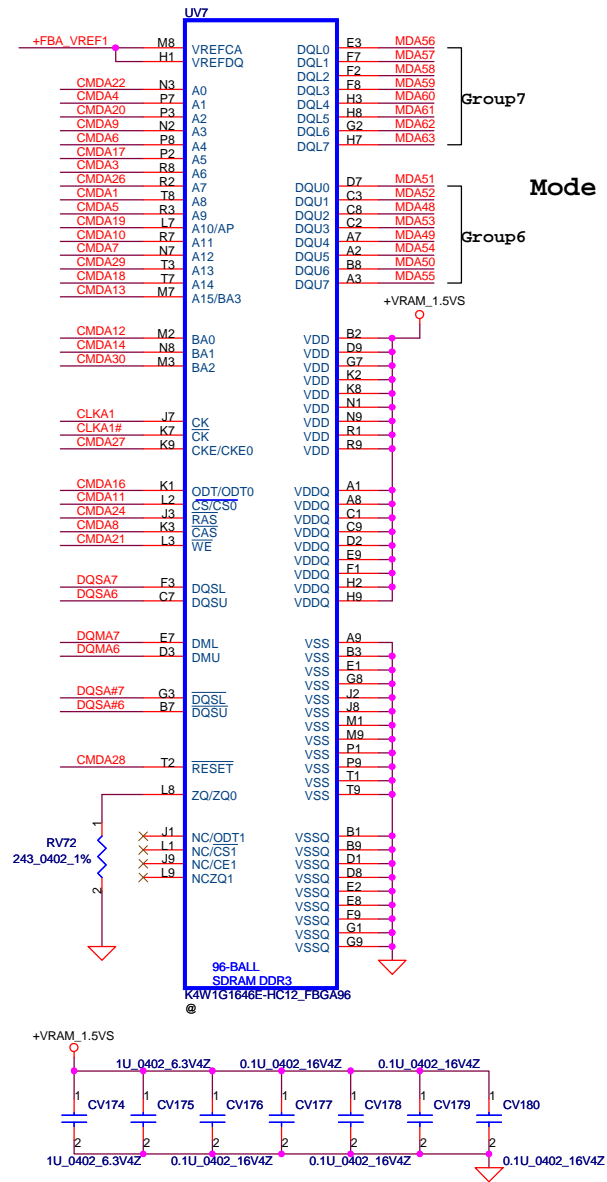
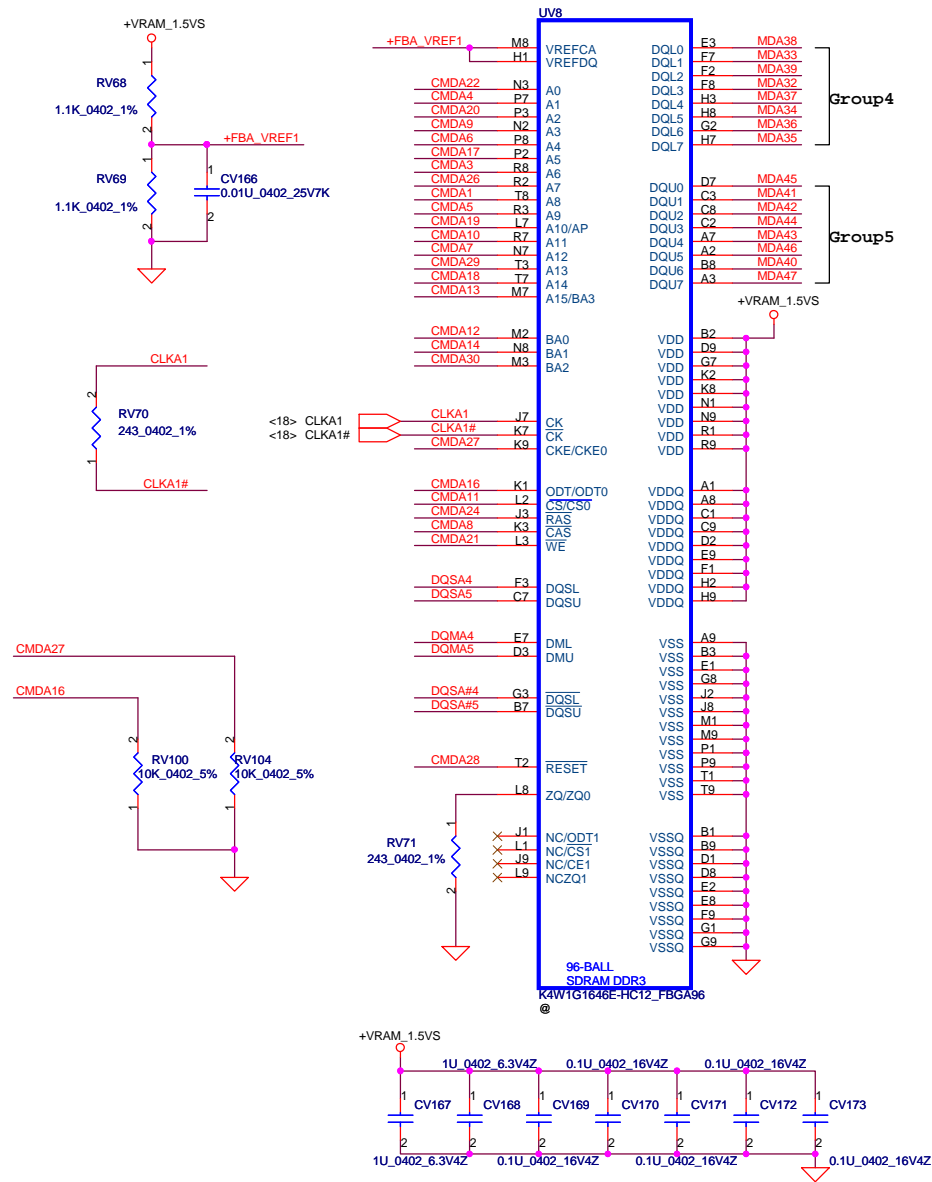


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				NWQAA LA-6062P M/B	2.0
				Date: Wednesday, March 24, 2010	Sheet 19 of 59

Memory Partition A - Lower 32 bits



Memory Partition A - Upper 32 bits

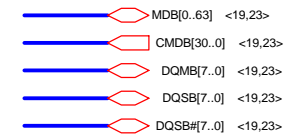
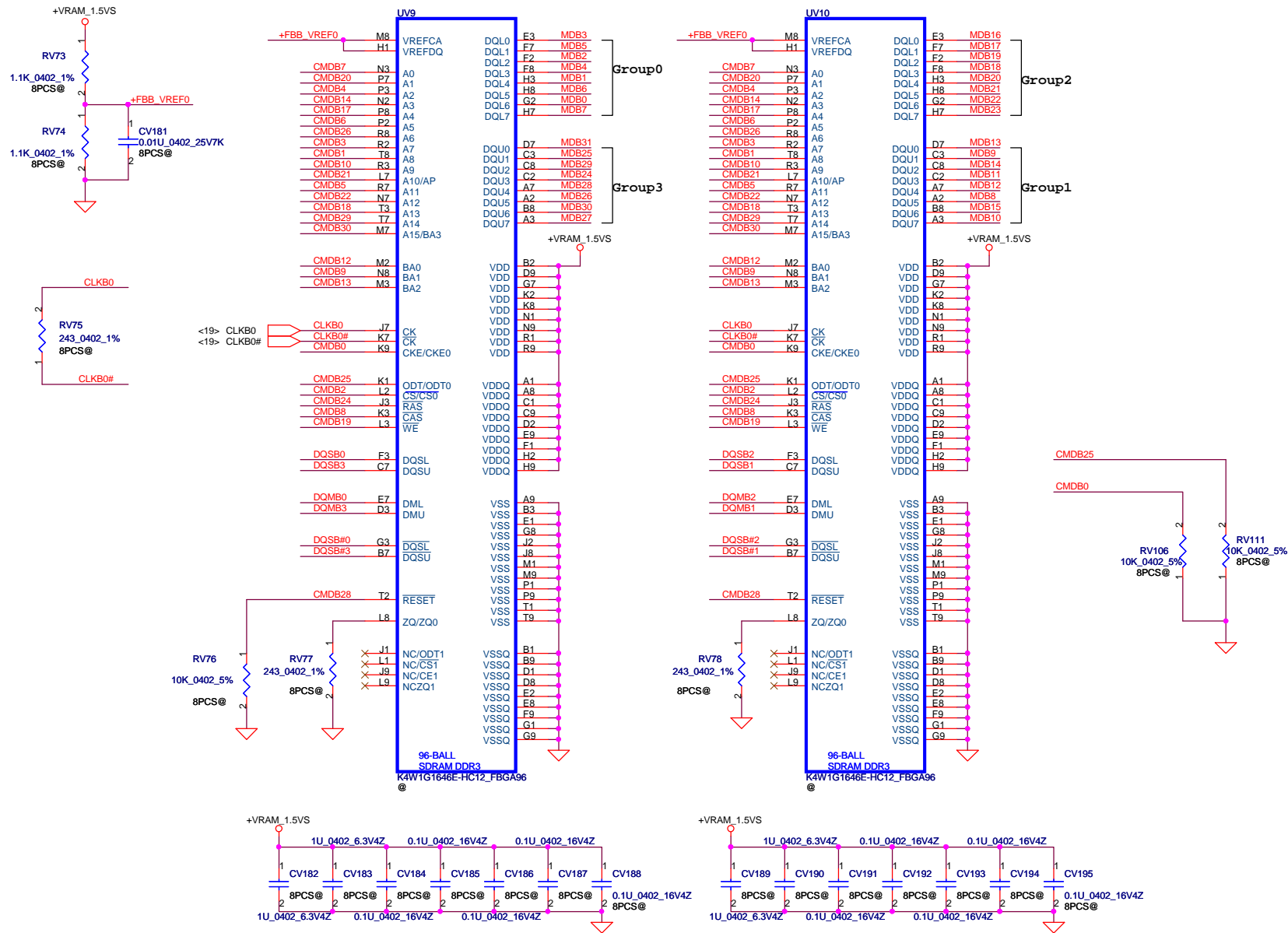


Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	VRAM A Upper	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 2.0
				NWQAA LA-6062P M/B	
				Date: Wednesday, March 24, 2010	Sheet 21 of 59

Memory Partition C - Lower 32 bits

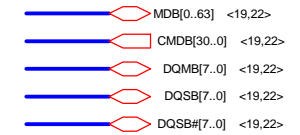
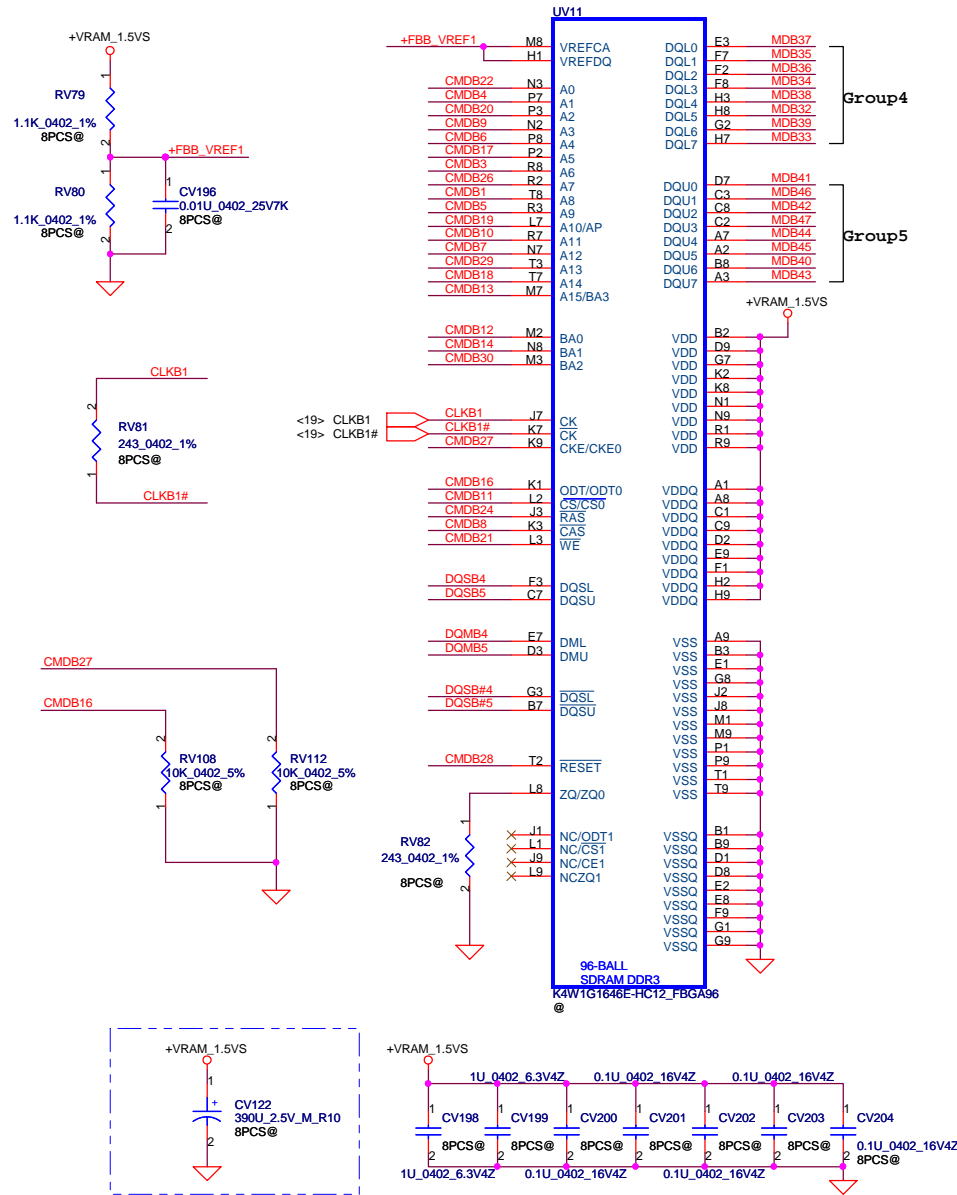


Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	VRAM C Lower	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				NWQAA LA-6062P M/B	2.0
				Date: Wednesday, March 24, 2010	Sheet 22 of 59

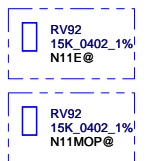
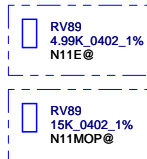
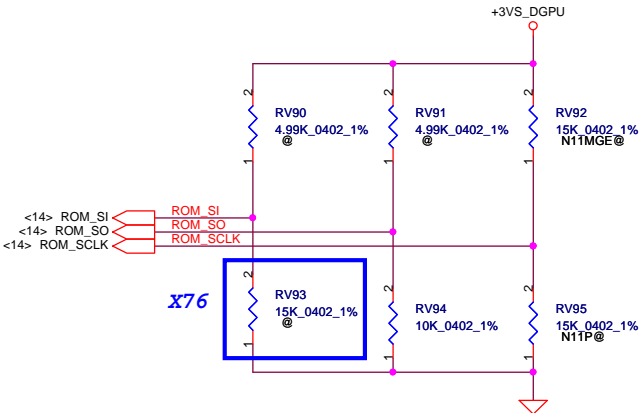
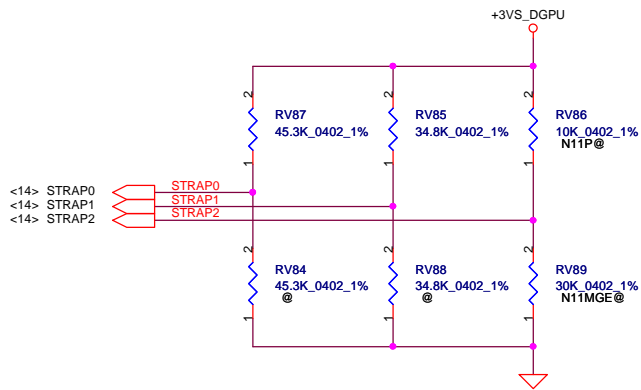
Memory Partition C - Upper 32 bits



Mode C - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD0	CKE_L	
CMD1	A8	A8
CMD2	CS0#_L	
CMD3	A7	A6
CMD4	A2	A1
CMD5	A11	A9
CMD6	A5	A4
CMD7	A0	A12
CMD8	CAS#	CAS#
CMD9	BA1	A3
CMD10	A9	A11
CMD11		CS0#_H
CMD12	BA0	BA0
CMD13	BA2	A15
CMD14	A3	BA1
CMD15		CS1#_H
CMD16		ODT_H
CMD17	A4	A5
CMD18	A13	A14
CMD19	WE#	A10
CMD20	A1	A2
CMD21	A10	WE#
CMD22	A12	A0
CMD23	CS1#_L	
CMD24	RAS#	RAS#
CMD25	ODT_L	
CMD26	A6	A7
CMD27		CKE_H
CMD28	RST	RST
CMD29	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/01	Deciphered Date	2010/01/01	VRAM C Upper	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				NWQAA LA-6062P M/B	2.0
				Date: Wednesday, March 24, 2010	Sheet 23 of 59



	DeviceID	ROM_SCLK	STRAP2
N11M-GE1	0xA75	Pull up 15K	Pull down 30K
N11P-GE1	0xA29	Pull down 15K	Pull up 10K
N11M-OP1	0xA72	Pull up 15K	Pull down 15K
N11E-GE1(LP)	0xCB0	Pull up 15K	Pull down 5K

Hynix H5TQ1G63BFR-12C SA000032400	512M	0010	PD 15K
	1G	0010	PD 15K
Samsung K4W1G1646E-HC12 SA000035700	512M	0011	PD 20K
	1G	0011	PD 20K

SD034150280

SD034200280

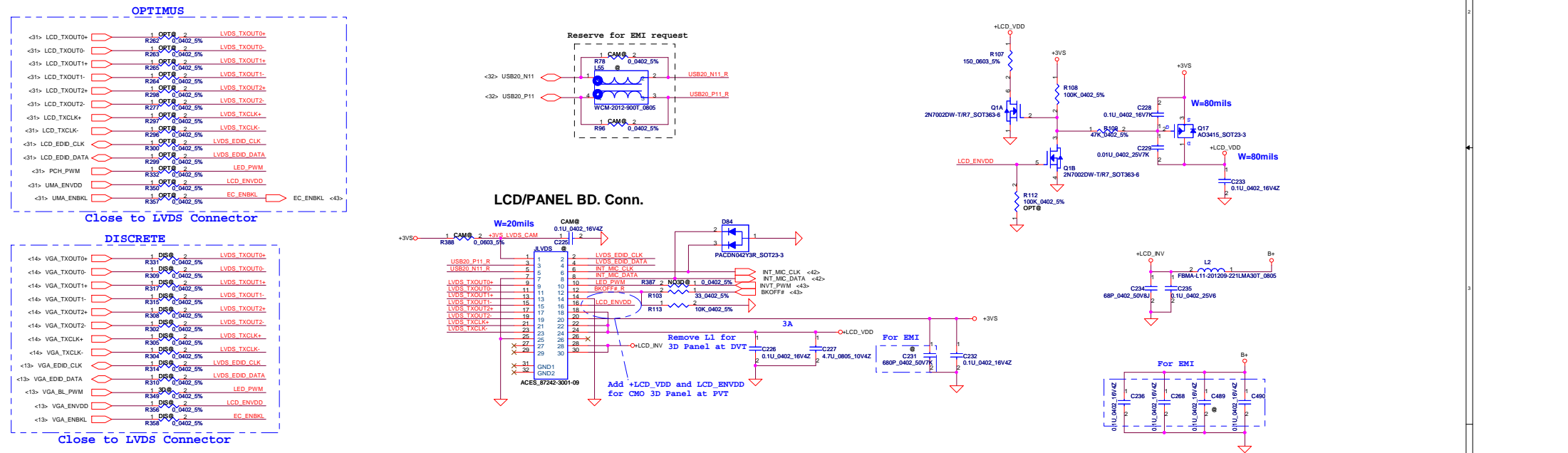
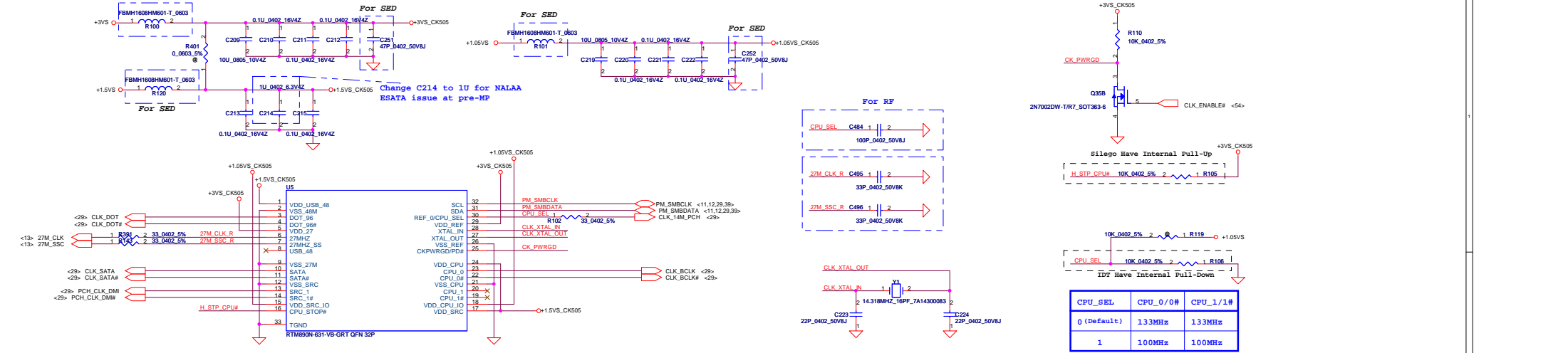
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR		XCLK_417	
0	No VBIOS ROM (Default)	0	277MHz (Default)
1	BIOS ROM is present	1	Reserved
FB_0_BAR_SIZE		USER Straps	
0	256MB (Default)	User[3:0]	
1	Reserved	1000-1100	Customer defined
3GIO_PADCFG		PEX_PLL_EN_TERM	
3GIO_PADCFG[3:0]		0	Disable (Default)
1110	Notebook Default	1	Enable
SLOT_CLOCK_CFG			
0	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		
SMBUS_ALT_ADDR		VGA_DEVICE	
0	0x9E (Default)	0	3D Device
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009/01/01	Deciphered Date	2010/01/01	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	NWQAA LA-6062P M/B	2.0
				Date:	Wednesday, March 24, 2010	Sheet 24 of 59

Clock Generator



OPTIMUS

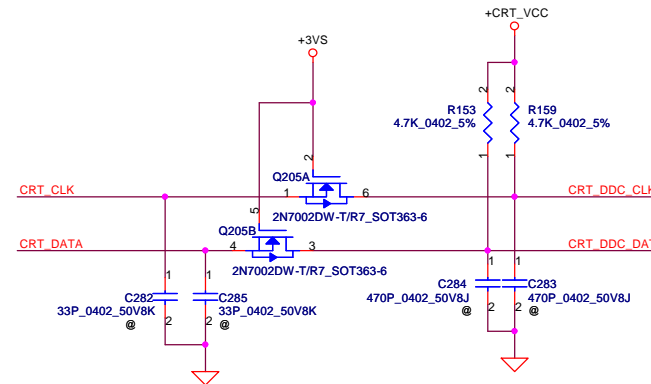
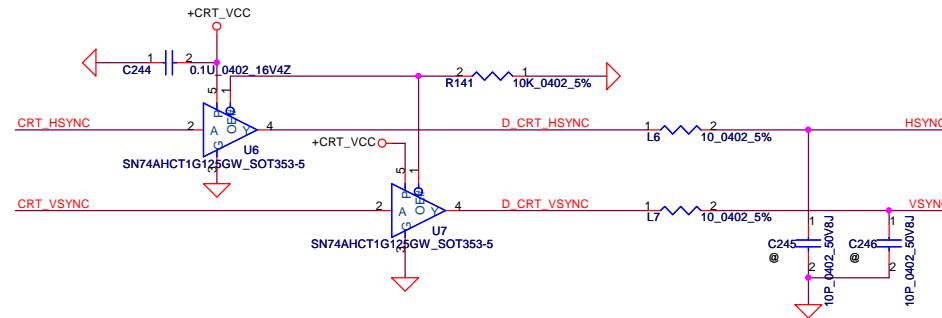
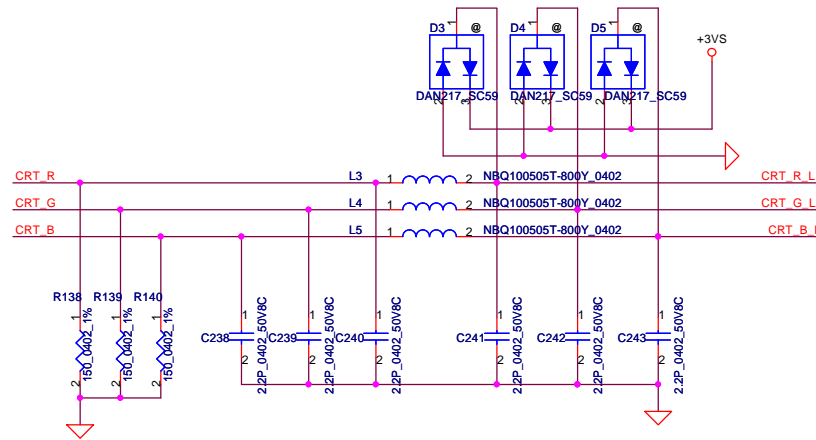
<31> UMA_CRT_R	1 OPT@ 2	CRT_R
<31> UMA_CRT_G	1 OPT@ 2	CRT_G
<31> UMA_CRT_B	1 OPT@ 2	CRT_B
<31> UMA_CRT_HSYNC	1 OPT@ 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT@ 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT@ 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT@ 2	CRT_DATA

Close to CRT Connector

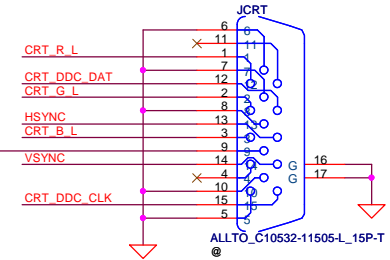
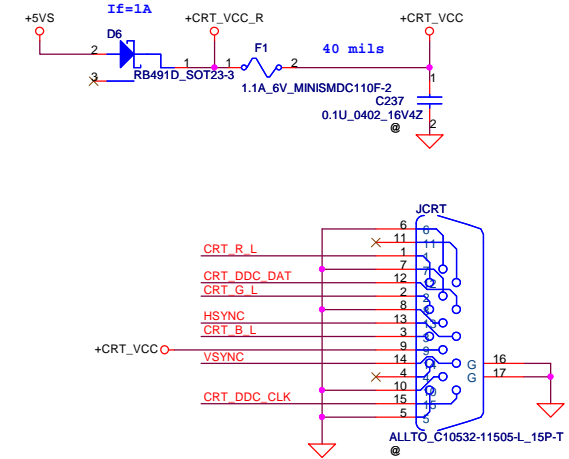
DISCRETE

<13> VGA_CRT_R	1 DIS@ 2	CRT_R
<13> VGA_CRT_G	1 DIS@ 2	CRT_G
<13> VGA_CRT_B	1 DIS@ 2	CRT_B
<13> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

Close to CRT Connector

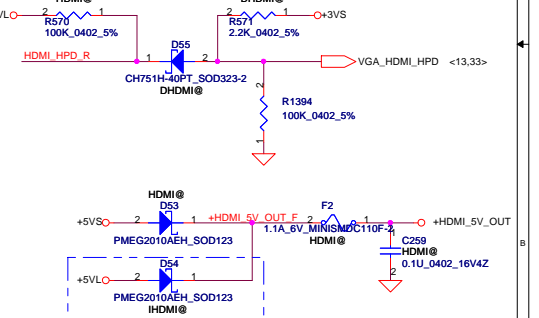
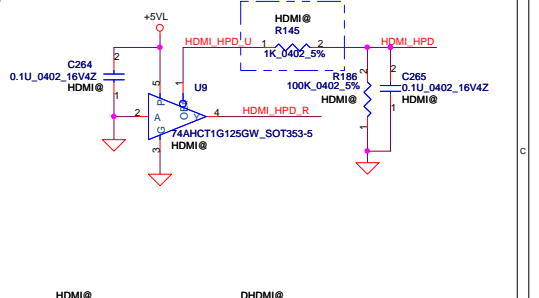
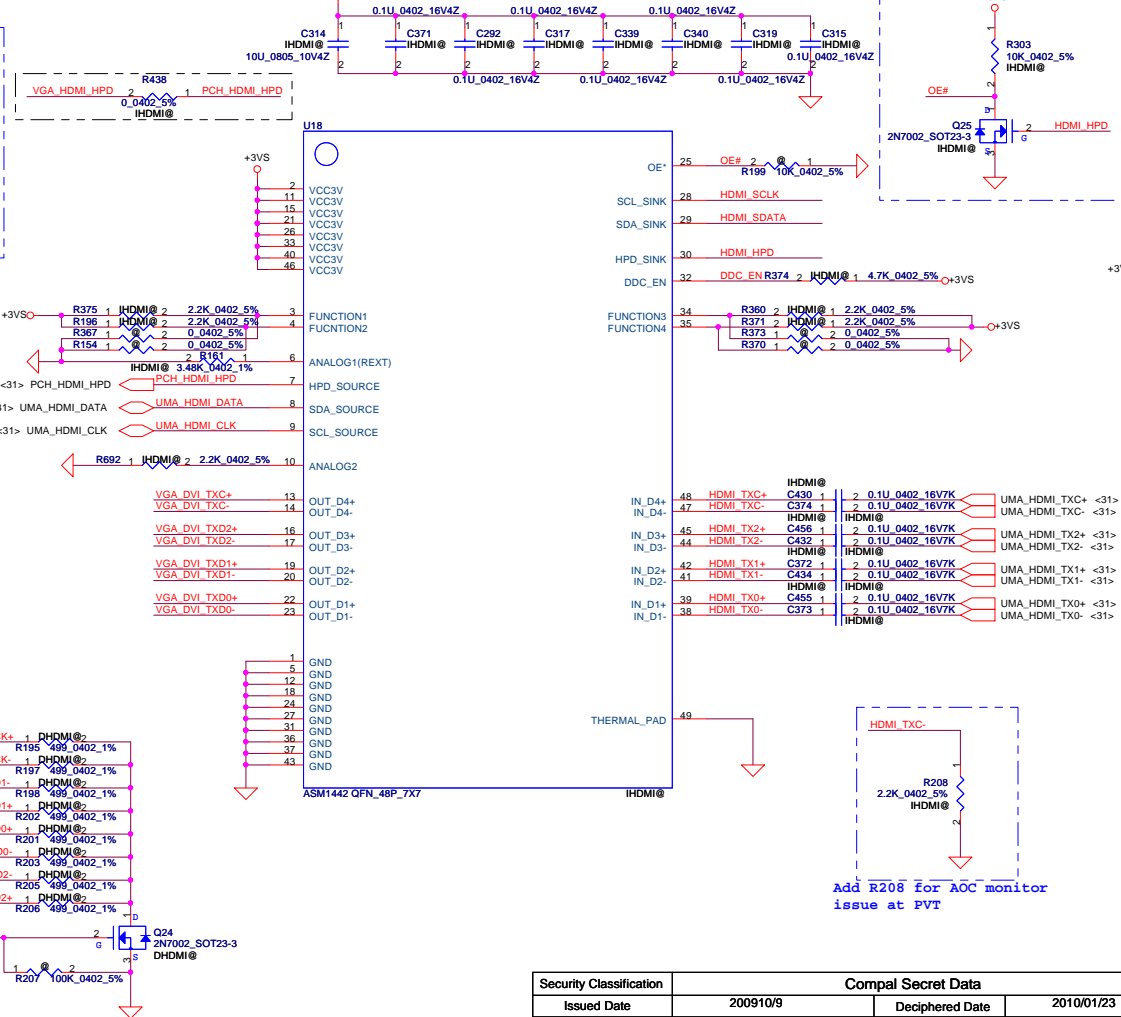
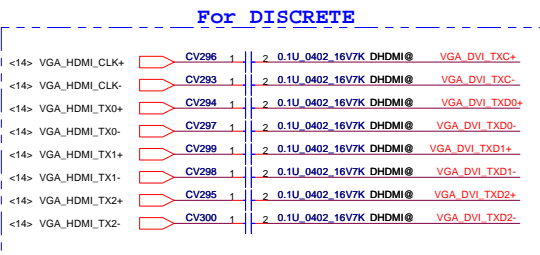
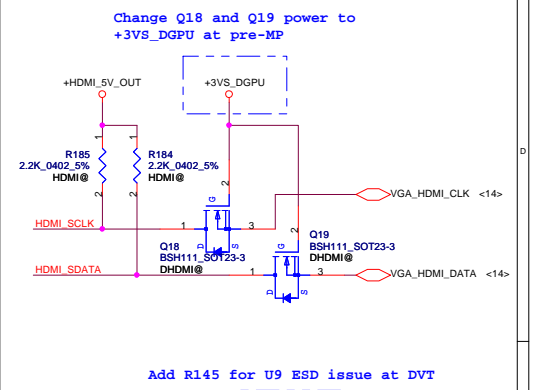
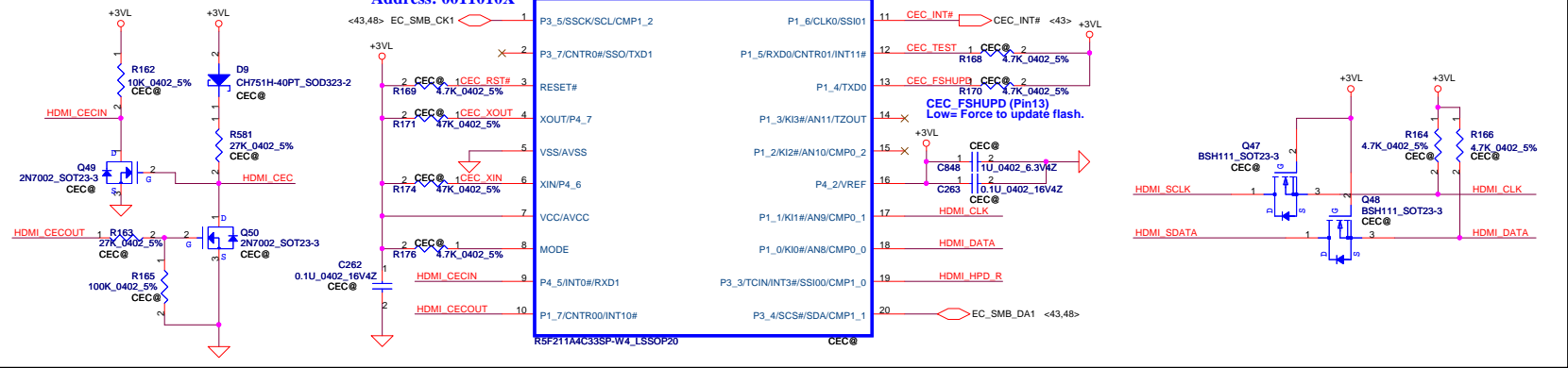


CRT CONNECTOR

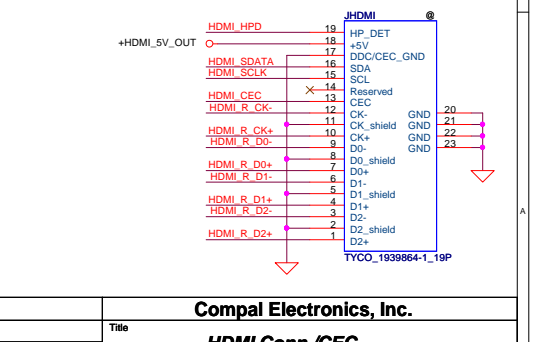


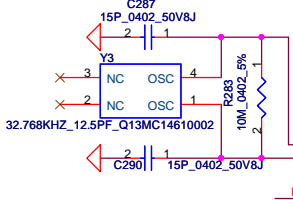
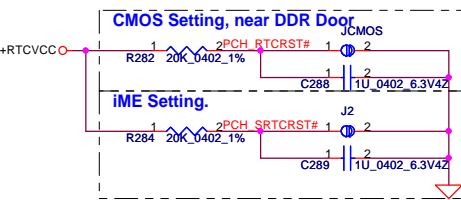
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CRT	
Size	Document Number	Rev		2.0	
Date	Wednesday, March 24, 2010	Sheet	26	of 59	

HDMI CEC Controller



HDMI Connector





Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN High - Enable Internal VRs (must be always pulled high)

HDA_SYNC

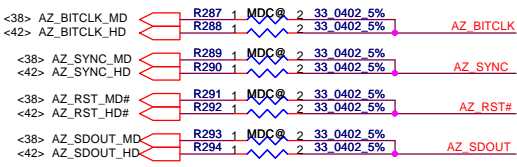
This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
L=>On Die PLL is supplied by 1.8V

HDA_SDO

This signal has a weak internal pull down.
This signal can't PU

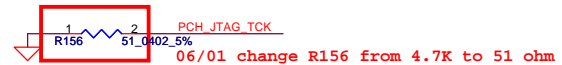
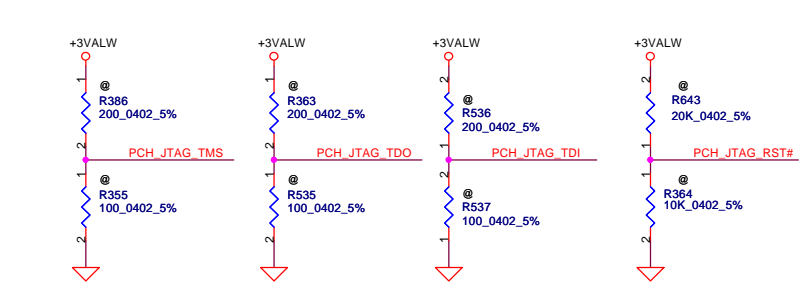
Flash Descriptor Security Override

HDA_DOCK_EN# Low = Enabled
High = Disabled *

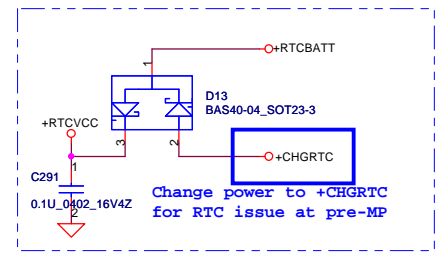
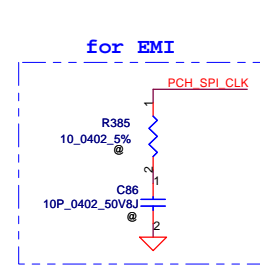
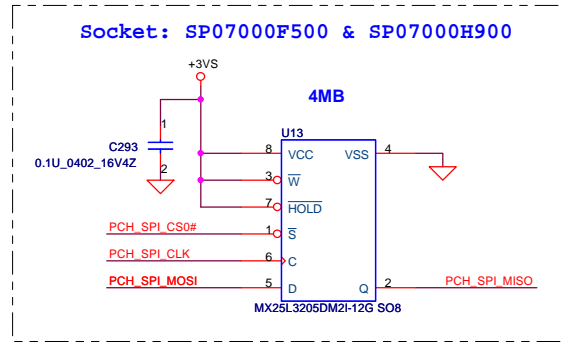
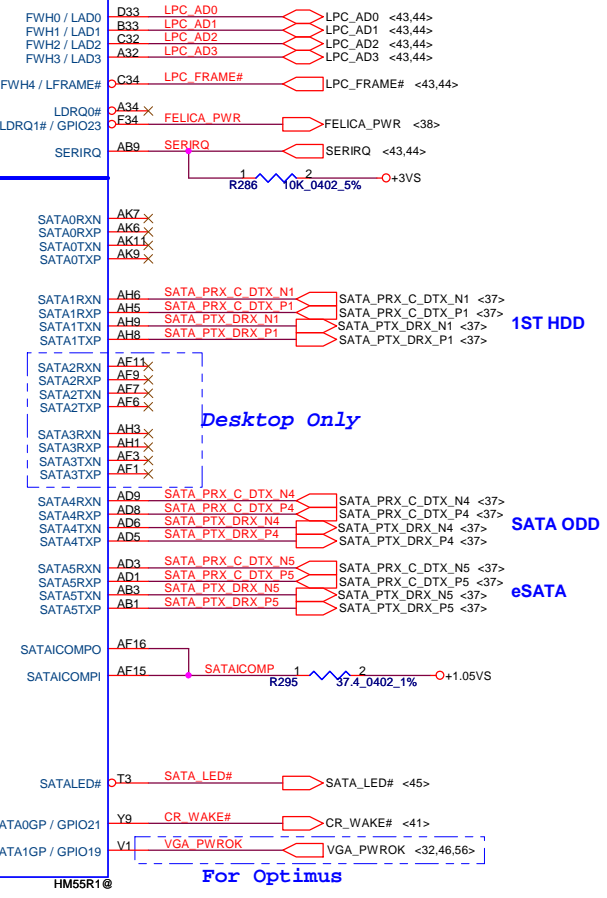
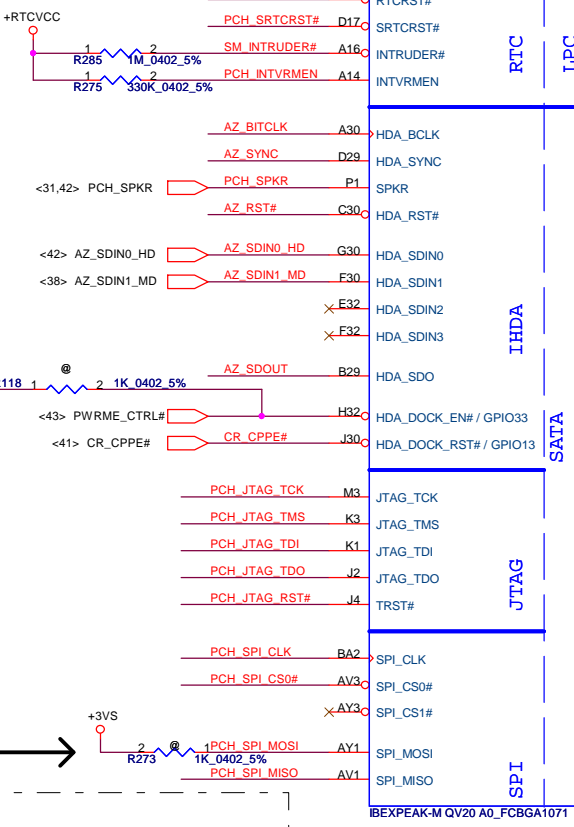


ITPM Enabled Internal: Pull down 20k

SPI_MOSI High = Enabled
Low = Disabled (Default)



PCH Pin	RefDes	PCH JTAG Enable	PCH JTAG Disable (Default)
PCH_JTAG_TDO	R358	No Install	No Install
PCH_JTAG_TMS	R355	No Install	No Install
PCH_JTAG_TDI	R354	No Install	No Install
PCH_JTAG_TCK	R156	No Install	No Install



Security Classification

Compal Secret Data

Issued Date

200910/9

Deciphered Date

2010/01/23

Title

Compal Electronics, Inc.

PCH_SPI/SATA/LPC/RTC/HDA

Size

B

Document Number

NWQAA LA-6062P M/B

Rev

2.0

Date

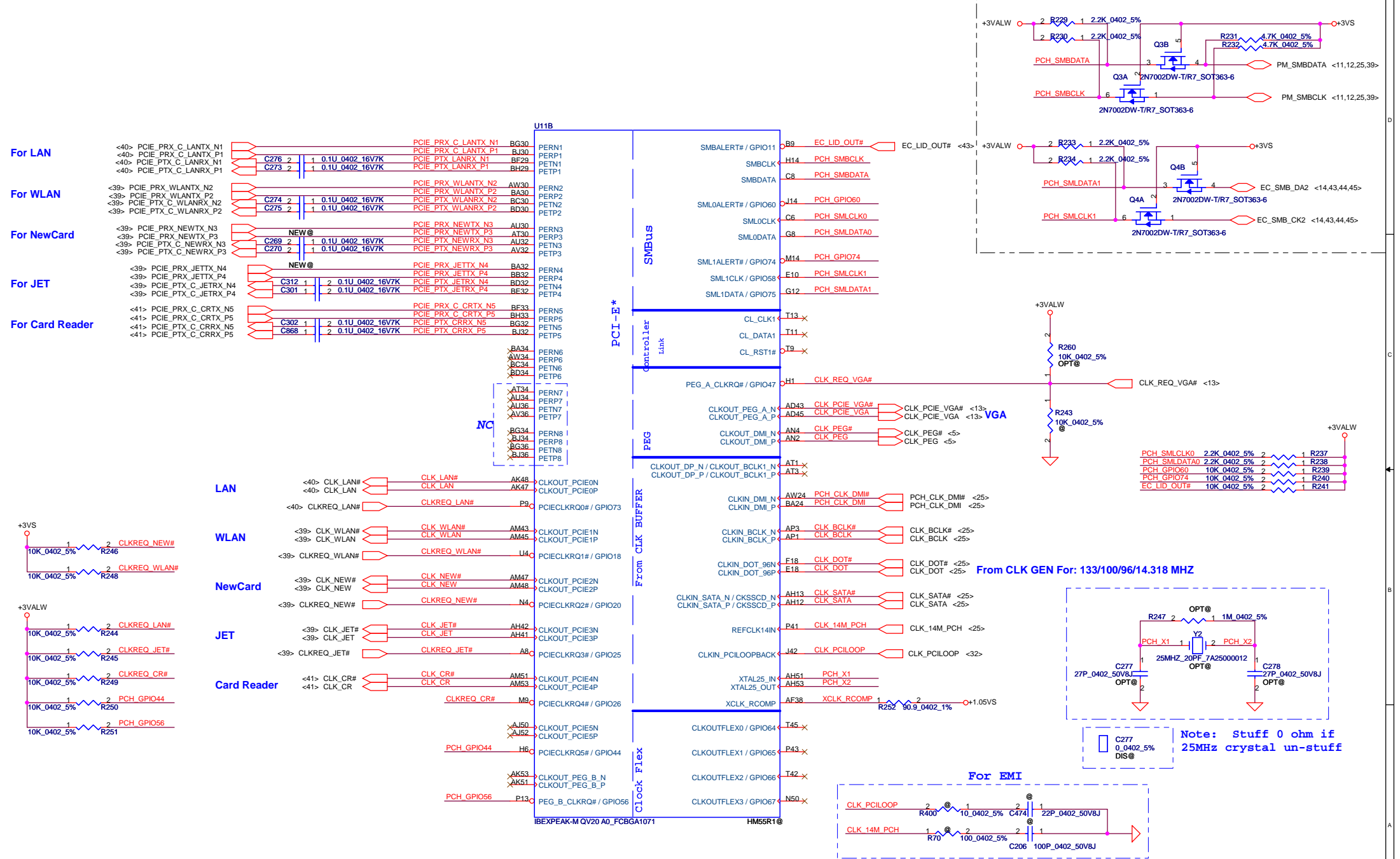
Wednesday, March 24, 2010

Sheet

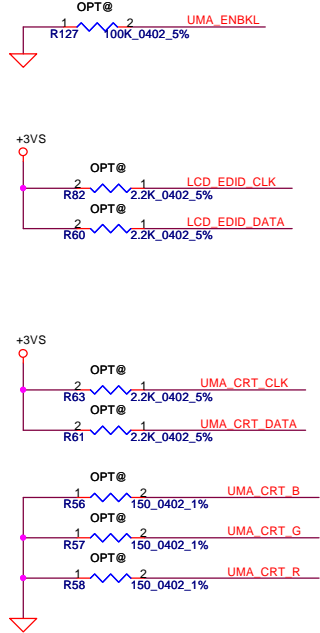
28

of

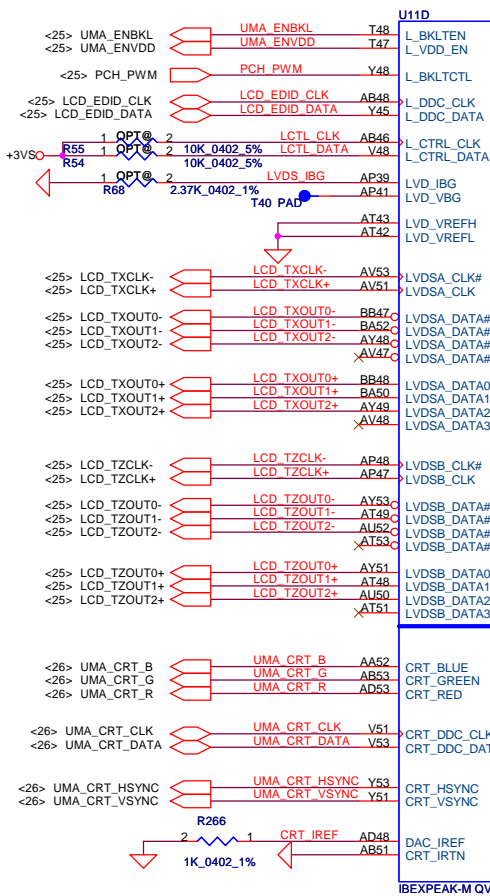
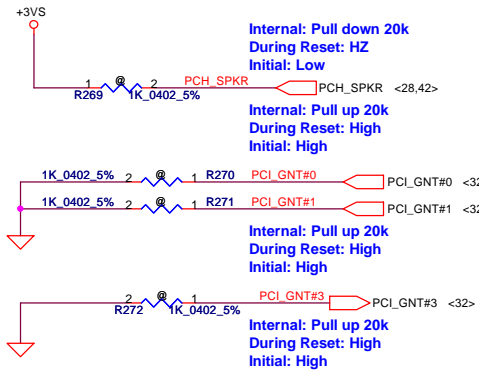
59



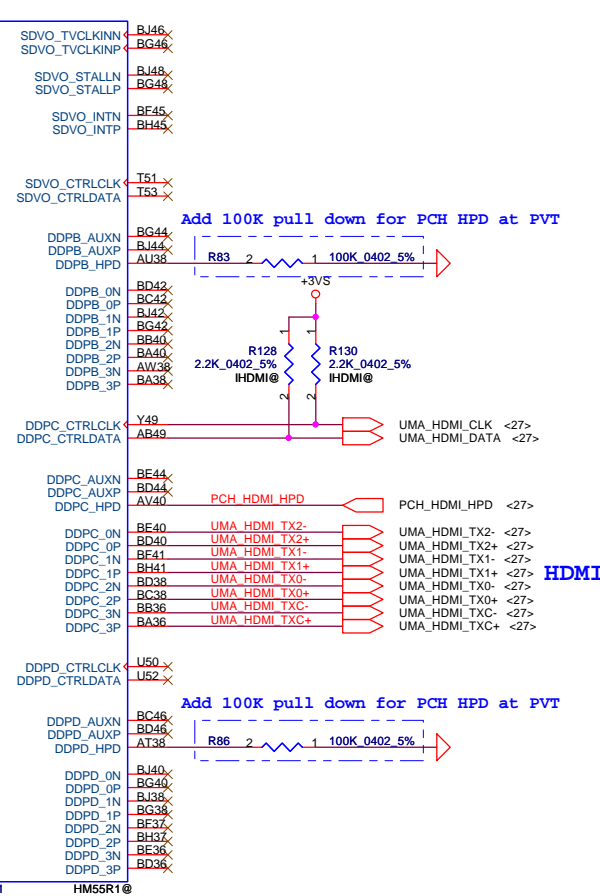
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	PCH CLK/PCIE/SMBUS	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				NWQAA LA-6062P M/B	2.0
				Date: Wednesday, March 24, 2010	Sheet 29 of 59



PCH Strap Pin



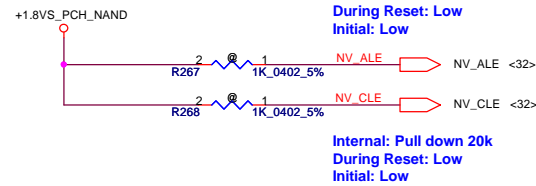
Digital Display Interface



NO REBOOT Strap		
PCH_SPKR	Low= Disable	High= Enable

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Location
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable
	High= A16 swap override Disable



Danbury Technology Enabled	
NV_ALE	High = Enabled
	Low = Disabled (Default)

DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default)
	High= Set to Vcc

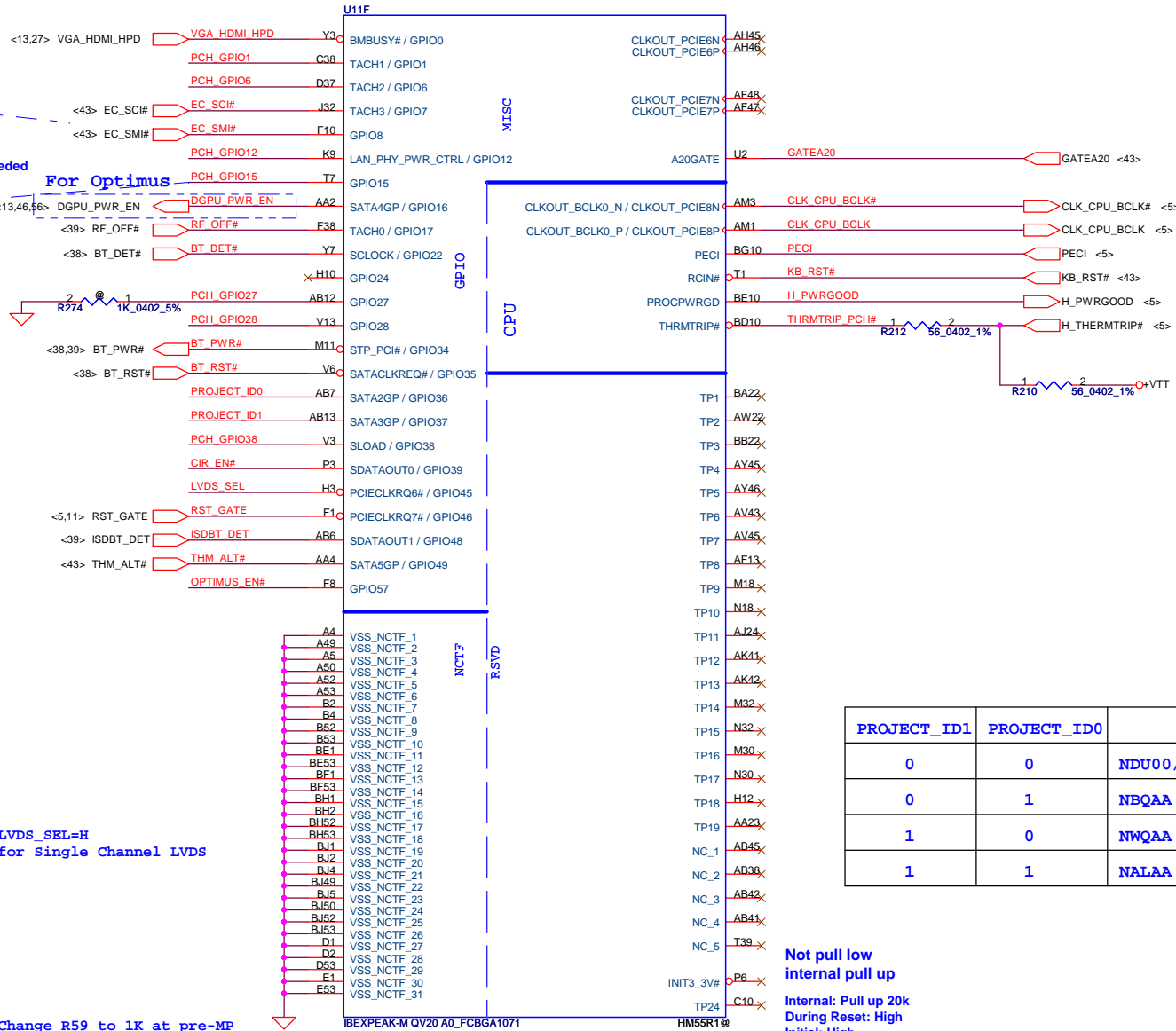
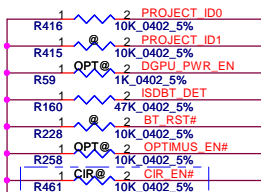
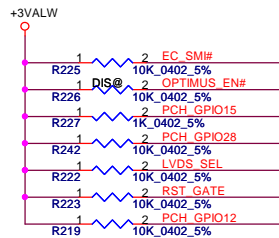
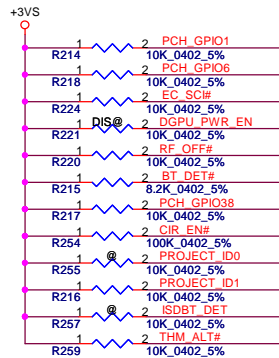
Security Classification		Compal Secret Data				Compal Electronics, Inc.									
Issued Date		200910/9		Deciphered Date		2010/01/23		Title							
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								PCH_CRT/LVDS/HDMI/STRAP							
								Size		Document Number			Rev		
								Custom		NWQAA LA-6062P M/B			2.0		
								Date:		Wednesday, March 24, 2010			Sheet 31 of 59		

GPIO8
Not pull down
Internal: Pull up 20k
During Reset: High
Initial: High

GPIO15
a Strong pull up may be needed
for GPIO Functionality
Internal: Pull down 20k
During Reset: Low
Initial: Low

On-Die PLL VR

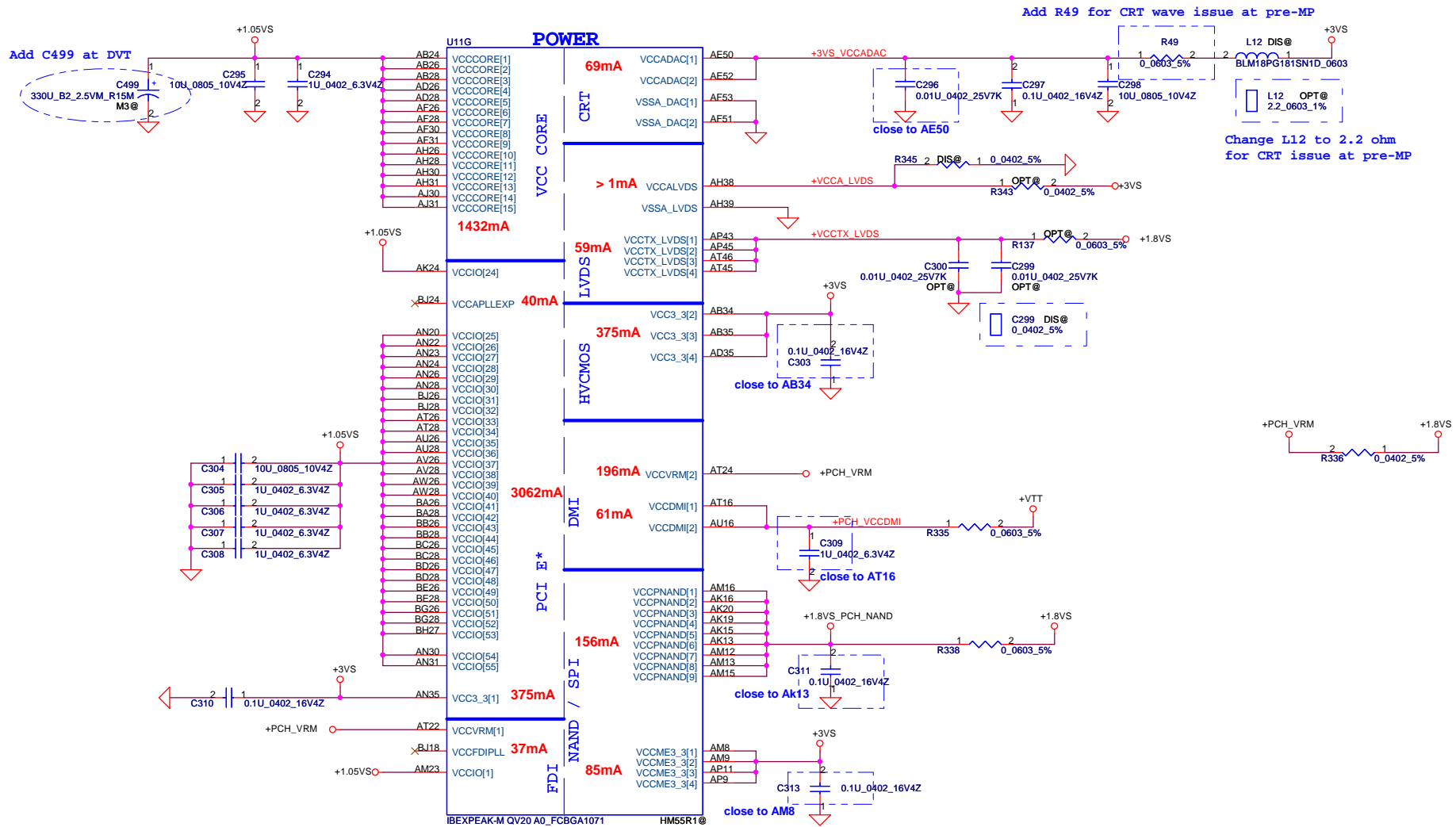
PCH_GPIO27 High = Enabled (Default)
Low = Disabled



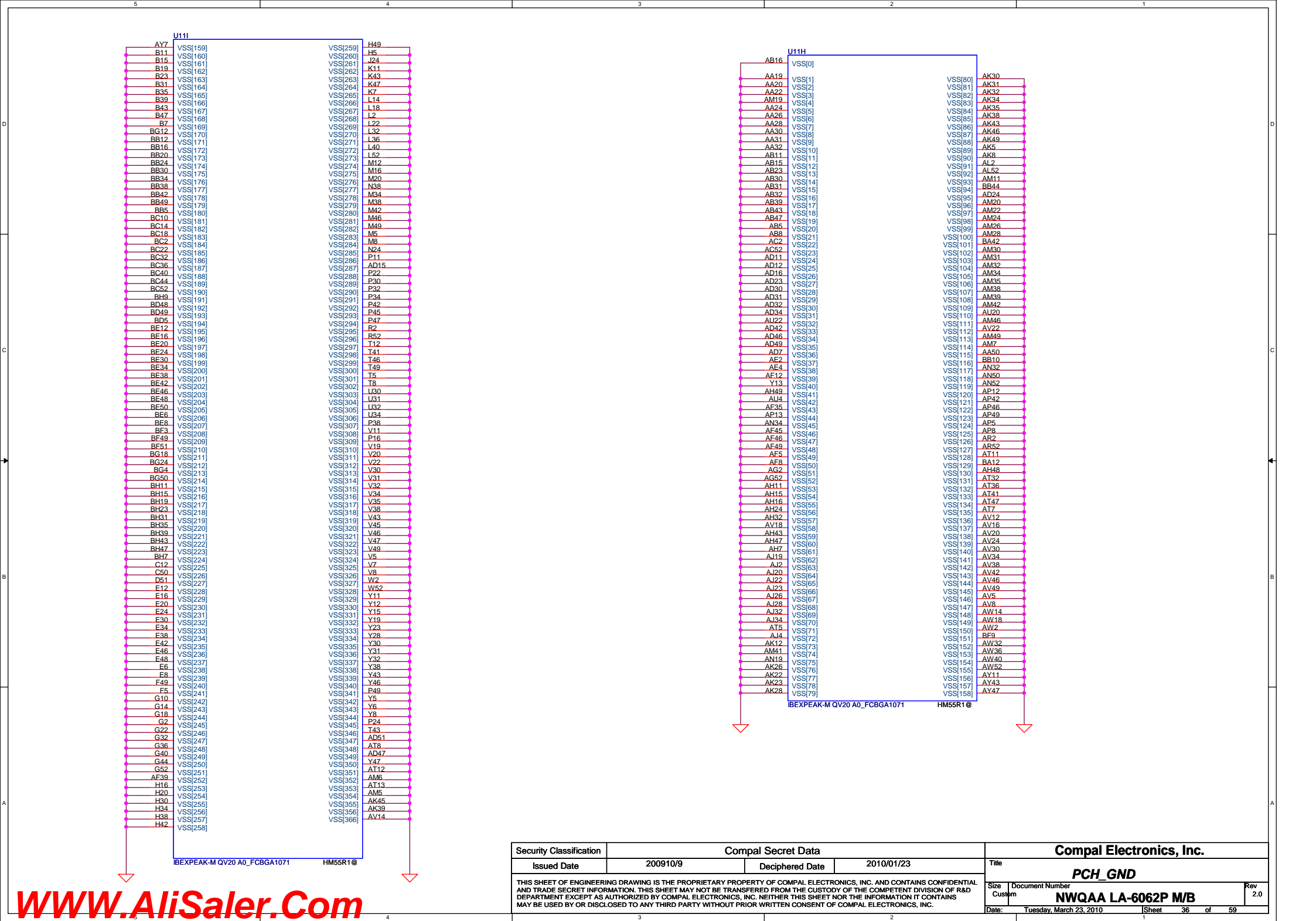
PROJECT_ID1	PROJECT_ID0	2010 Project ID setting
0	0	NDU00/10 (Streamline-M/-S 11.6/13.3")
0	1	NBQAA (Bordeaux 14")
1	0	NWQAA (Marseille 16")
1	1	NALAA (Hamburg 17.3")

Add OPTIMUS_EN# at DVT		
OPTIMUS_EN#	H	L
SKU	Discrete	Optimus

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCH_CPU/GPIO	
Size B	Document Number	Rev 2.0		Date: Wednesday, March 24, 2010	
NWQAA LA-6062P M/B		Sheet 33 of 59			

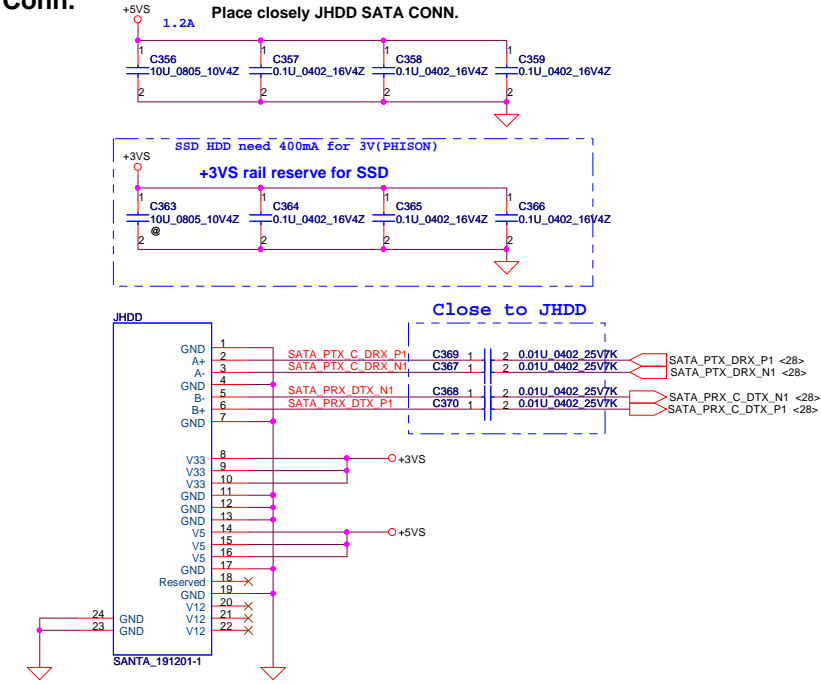


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCH_POWER-1	
Size B	Document Number	NWQAA LA-6062P M/B		Rev	2.0
Date:	Tuesday, March 23, 2010	Sheet	34	of	59

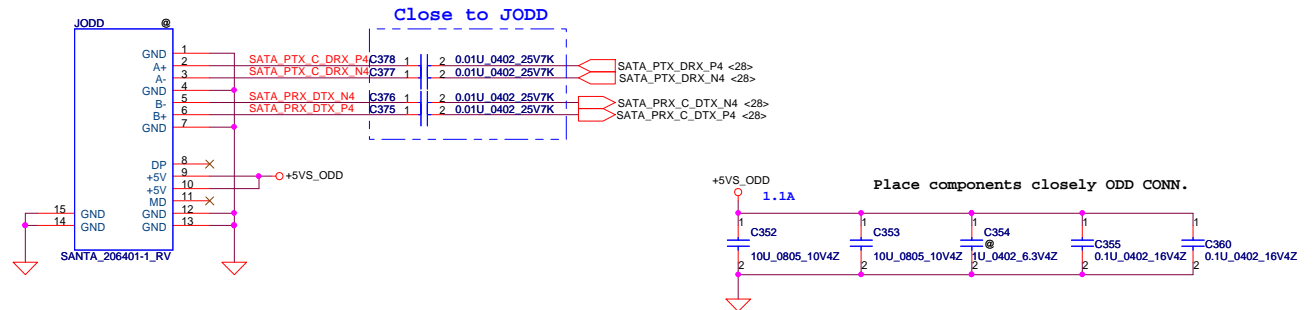


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PCH_GND	
Size	Document Number	Rev		2.0	
Custom	NWQAA LA-6062P M/B				
Date:	Tuesday, March 23, 2010	Sheet	36	of	59

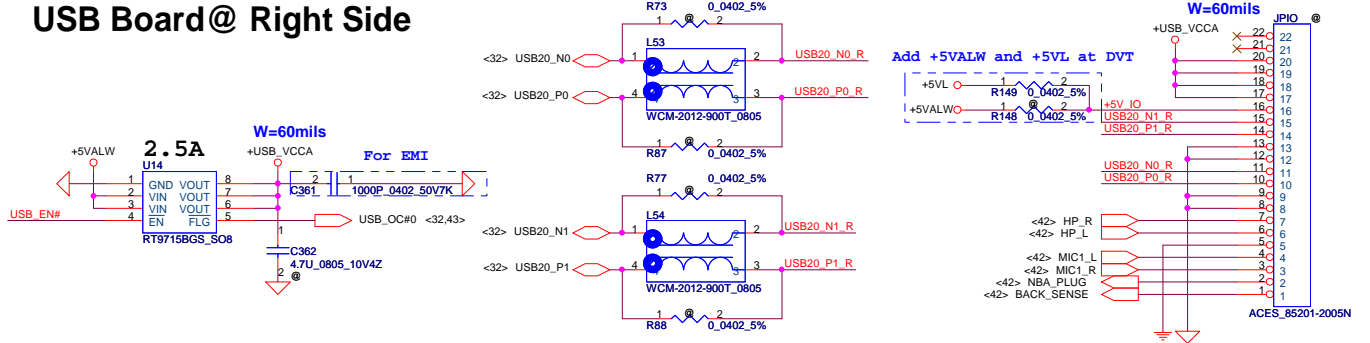
SATA HDD Conn.



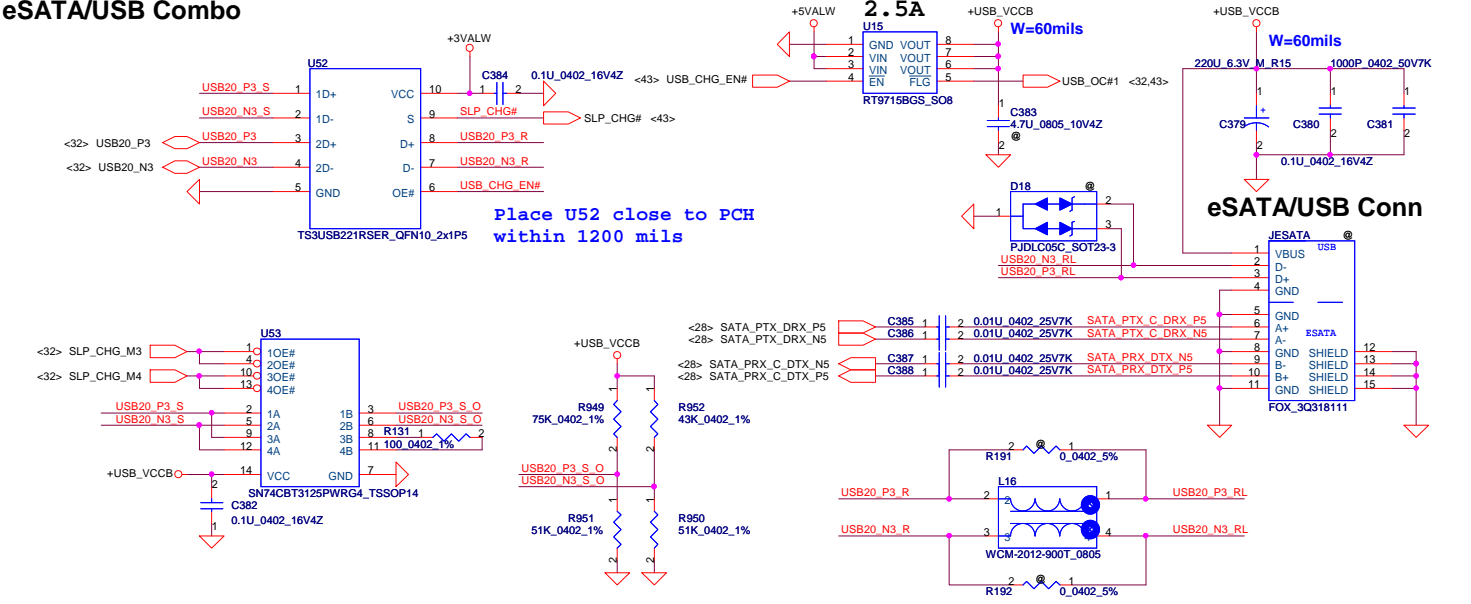
SATA ODD Conn



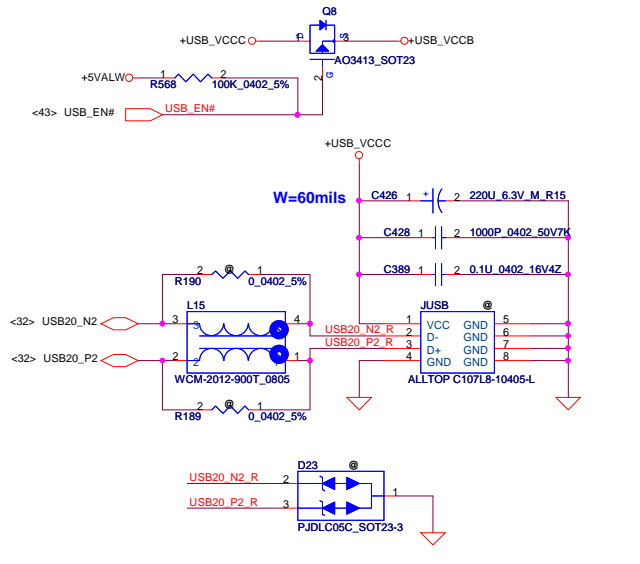
USB Board@ Right Side



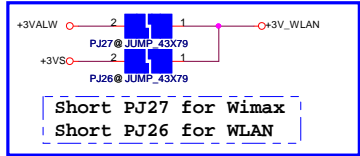
eSATA/USB Combo



USB Board@ Left Side



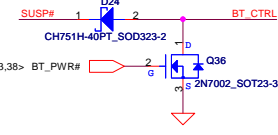
Slot 1 Half PCIe Mini Card-WLAN/ WiMax



WLAN&BT Combo module circuits

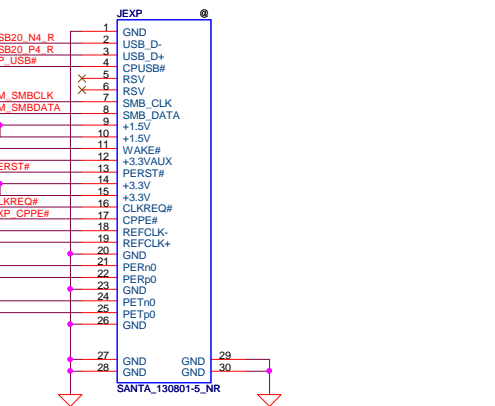
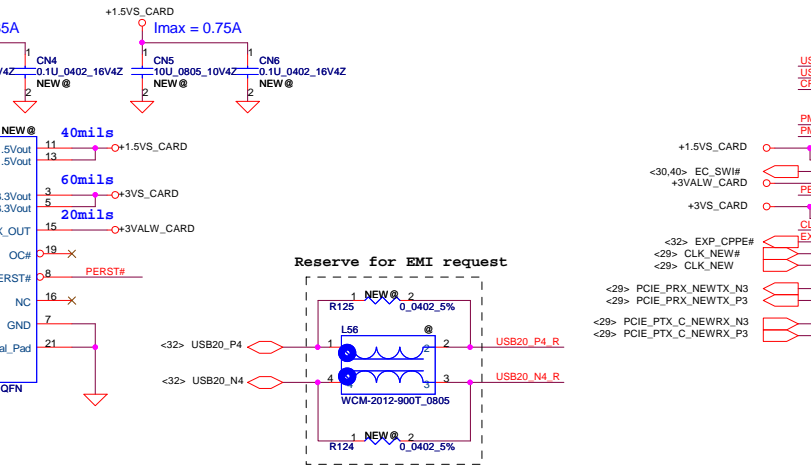
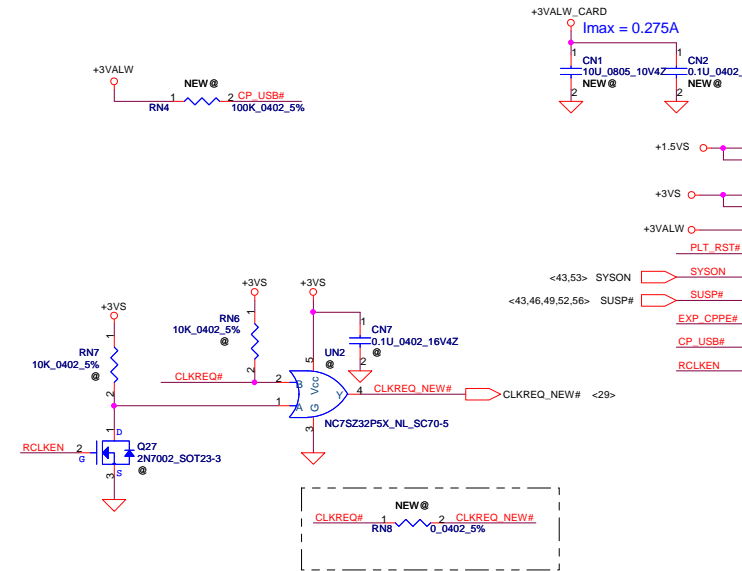
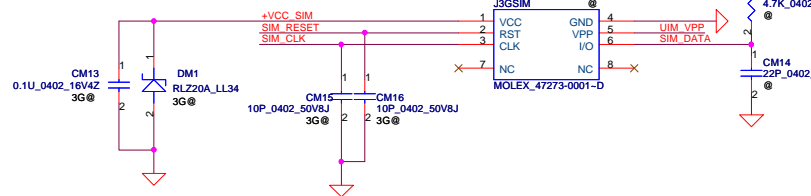
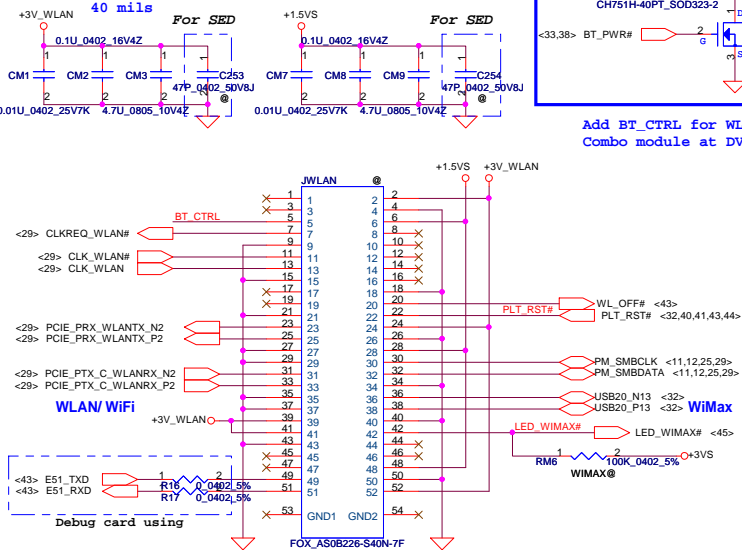
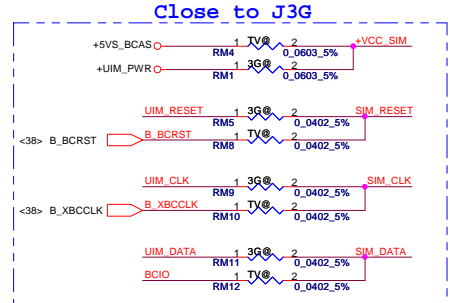
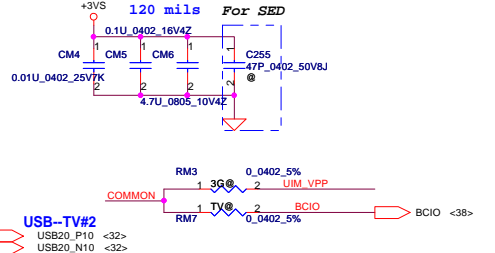
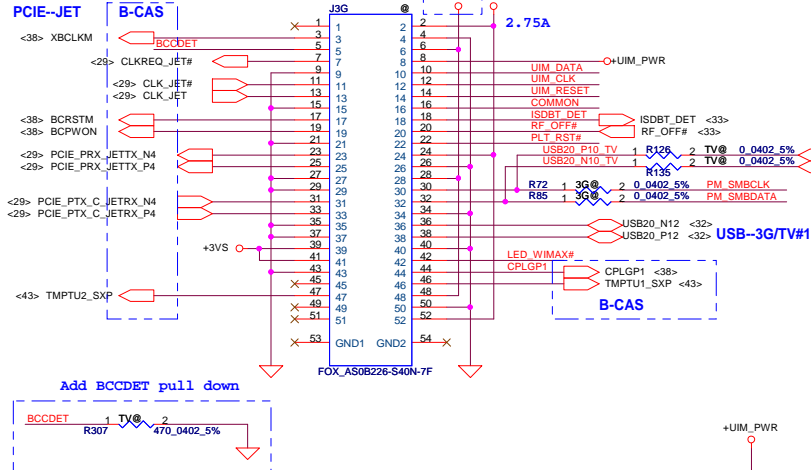
	BT on module	BT on module
BT_CTRL	Enable	Disable
BT_PWR#	L	H

**If +3V_WLAN is +3VS, please remove D24

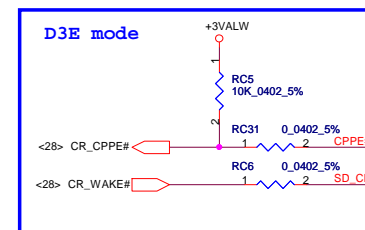
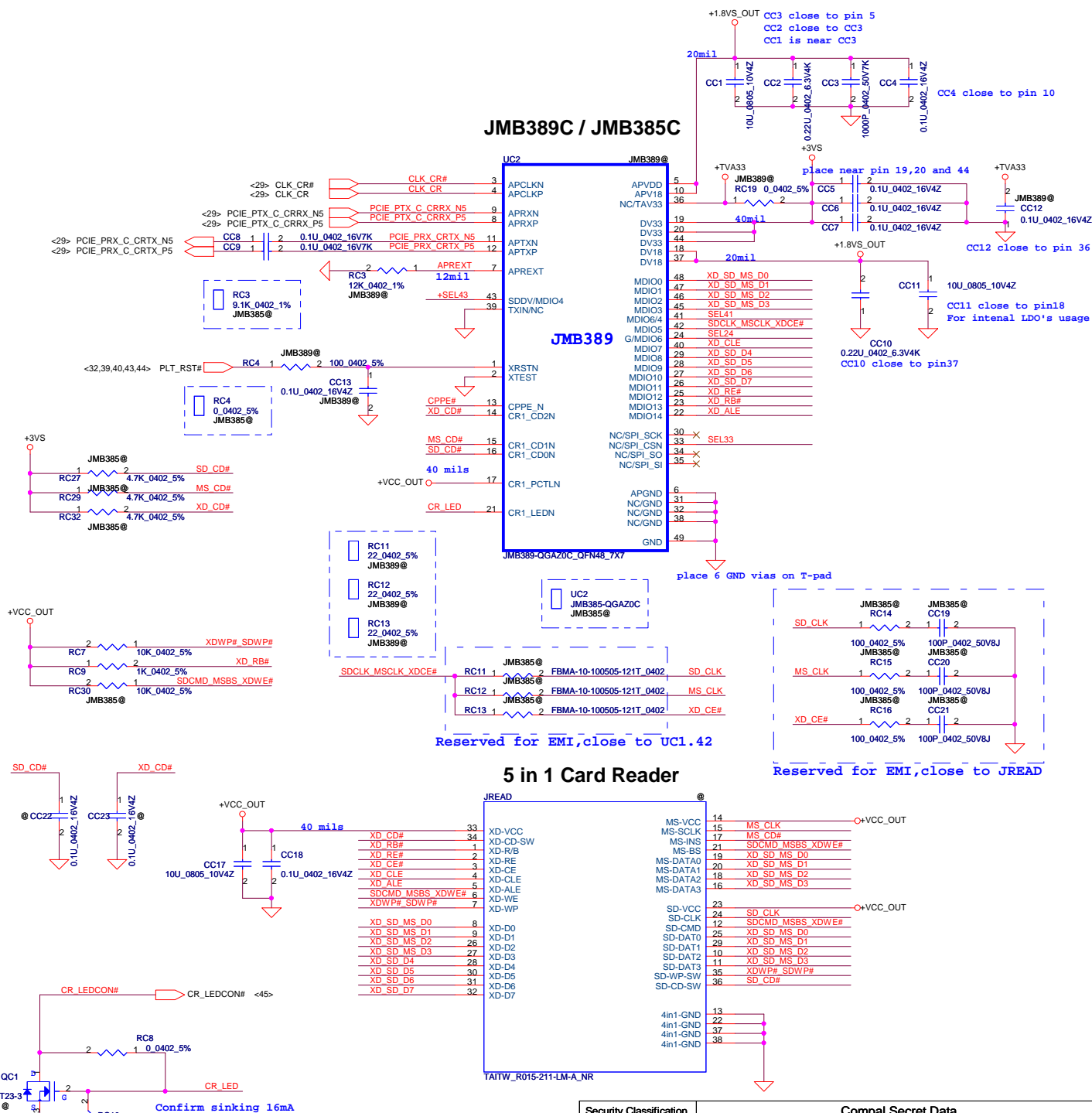


Add BT_CTRL for WLAN & BT Combo module at DVT

Slot 2 Full PCIe Mini Card- 3G/ TV Tuner Half PCIe Mini Card- JET

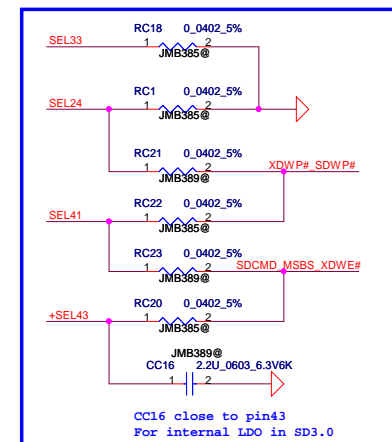


Security Classification	Compal Secret Data	2010/01/23	Title	
Issued Date	Deciphered Date	2010/01/23	PCle-WLAN/JET/3G/TV/NewCard	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size	Document Number
			Rev	2.0
			Date:	Wednesday, March 24, 2010
			Sheet	39 of 59

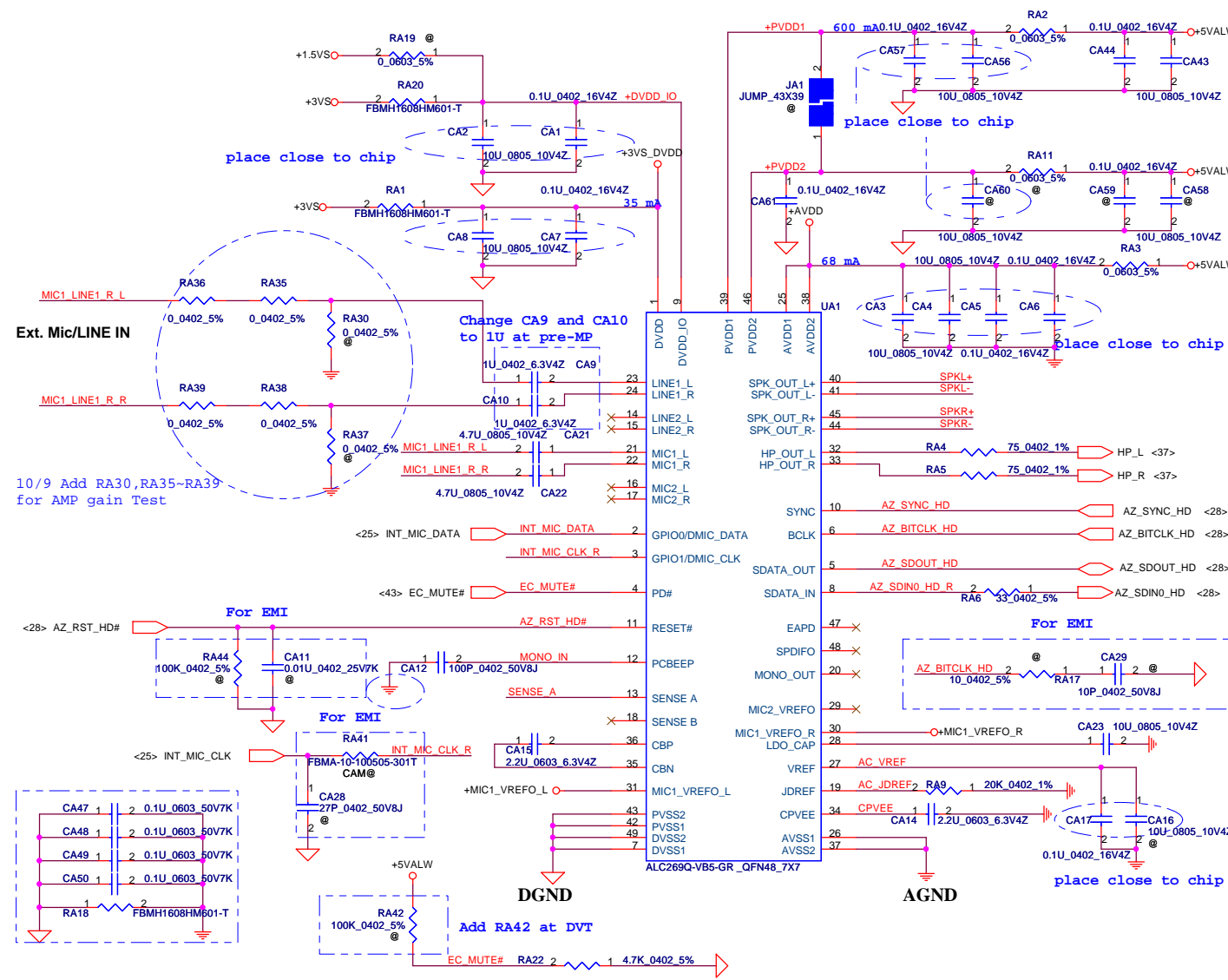


Power On Strapping setting		
Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO14	CR_LED high active	CR_LED low active★

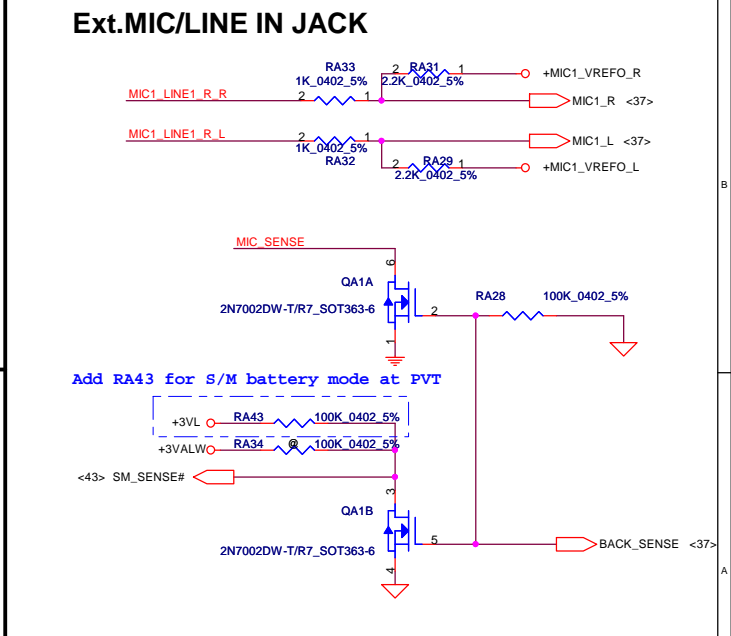
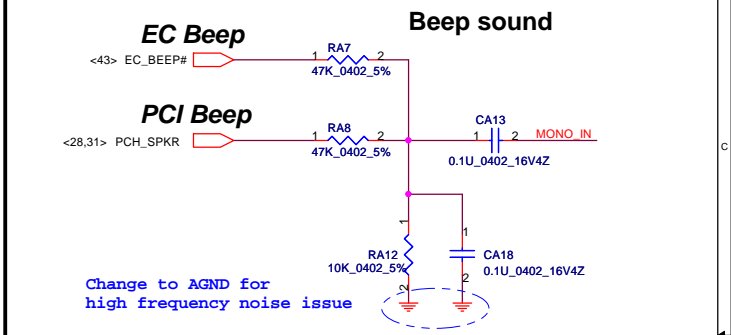
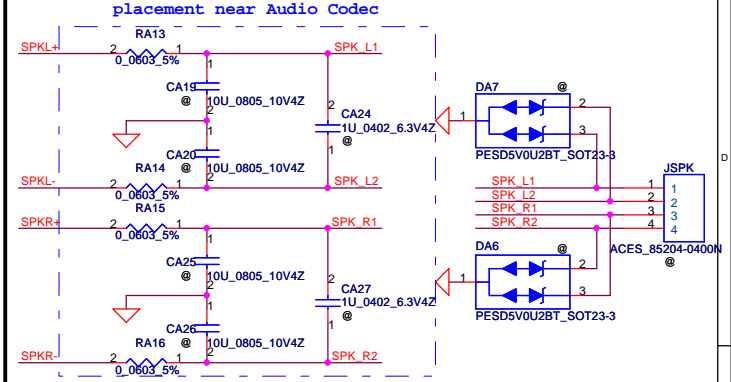
The diagram illustrates the power-on strapping configuration for MDIO7 and MDIO14. Both pins are connected to a +3VS supply through 10K_0402_5% resistors. MDIO7 is connected to pin 1 of RC28 (XD_CLE) and pin 2 to the resistor. MDIO14 is connected to pin 1 of RC26 (XD_ALE) and pin 2 to the resistor. Additionally, MDIO14 is connected to pin 1 of RC25 and pin 2 to a 200K_0402_5% resistor, which is connected to ground.



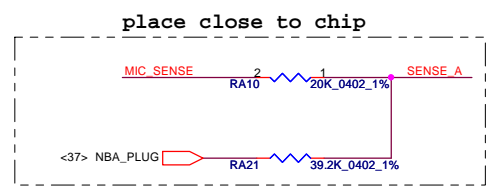
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	200910/9	Deciphered Date	2010/01/23	Card Reader JMB385/389		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		
				Size	Document Number	Rev
				Custom	NWQAA LA-6062P M/B	2.0
Date:		Wednesday, March 24, 2010		Sheet	41	of 59



Speaker Connector



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

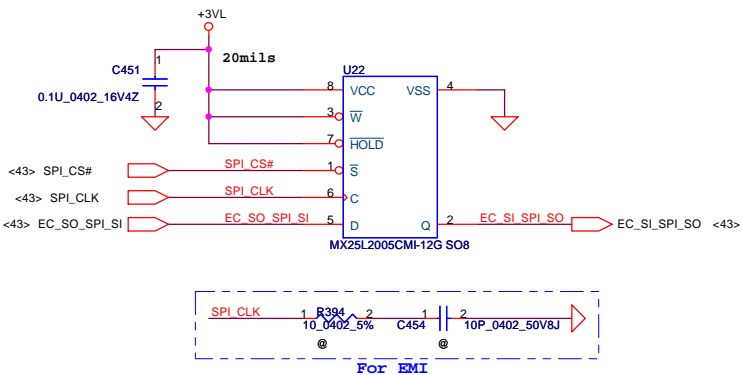


Security Classification		Compal Secret Data		Title	
Issued Date	200910/9	Deciphered Date	2010/01/23	Size	Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 2.0	
				Date:	Wednesday, March 24, 2010
				Sheet	42 of 59

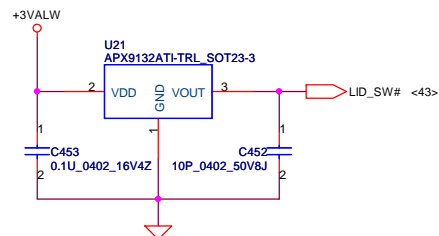


Security Classification		Compal Secret Data		Compal Electronics, Inc. ENE-KB926 RevD2		
Issued Date	2009/10/9	Deciphered Date	2010/01/23	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
					NWQAA LA-6062P M/B	2.0
				Date:	Wednesday, March 24, 2010	Sheet 43 of 59

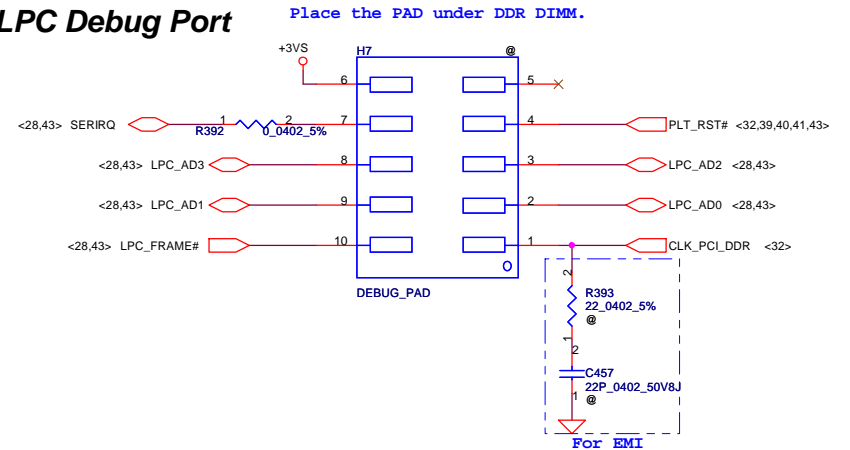
SPI Flash (256KB)



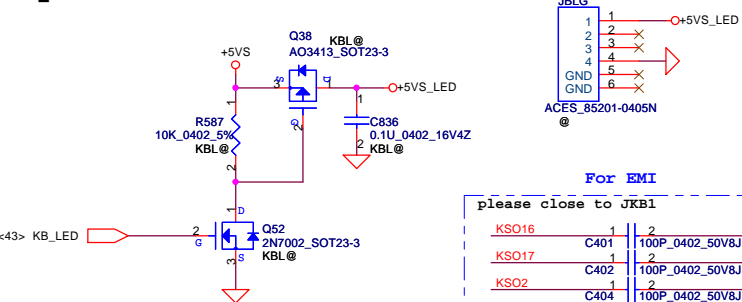
Lid SW



LPC Debug Port



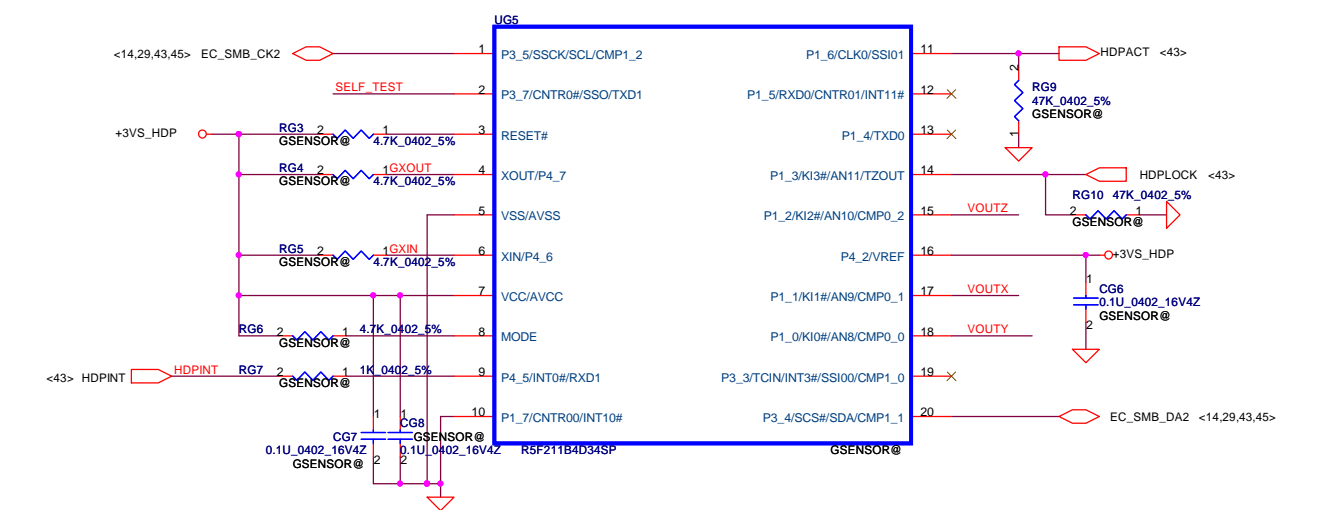
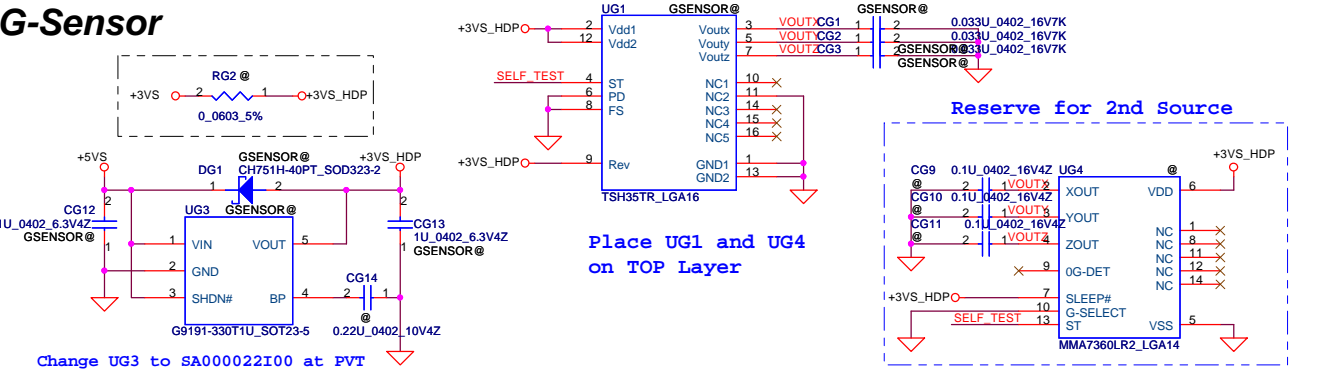
Keyboard LED



KEYBOARD CONN.

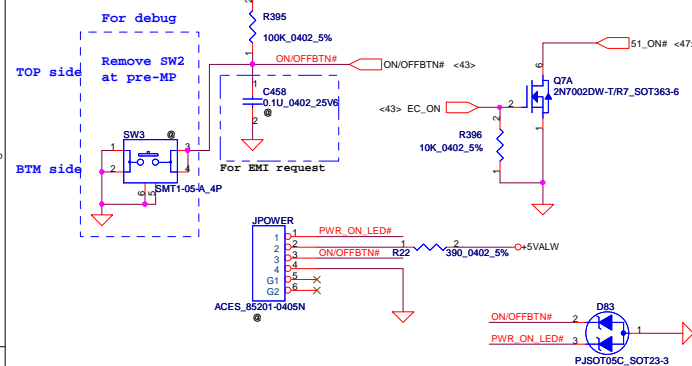


G-Sensor

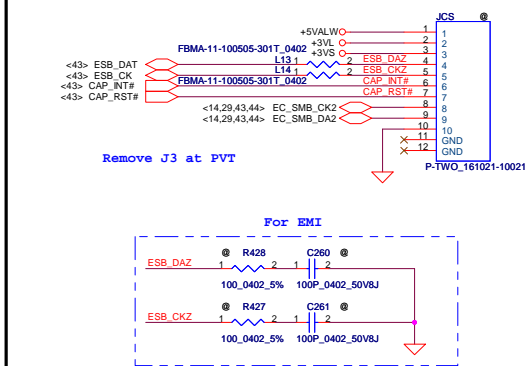


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SPI ROM/LID/Debug/KB/G-Sen
Size	Document Number	Rev		2.0
Date:	Wednesday, March 24, 2010	Sheet	44	of 59

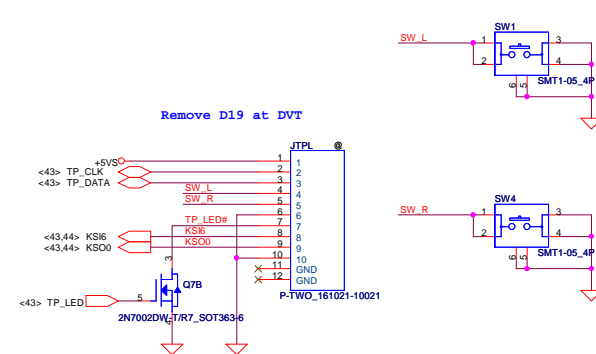
Power Button



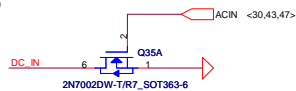
Caps Sensor/Light Sensor Conn.



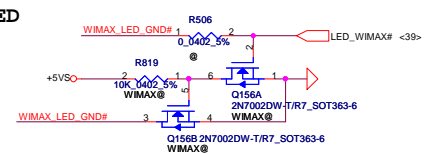
Touchpad & Light Pipe Connector



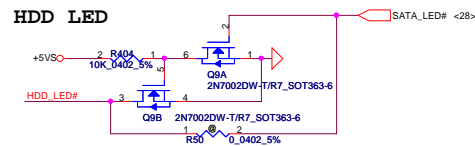
DC-IN LED



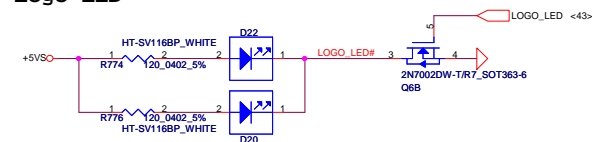
WiMAX LED



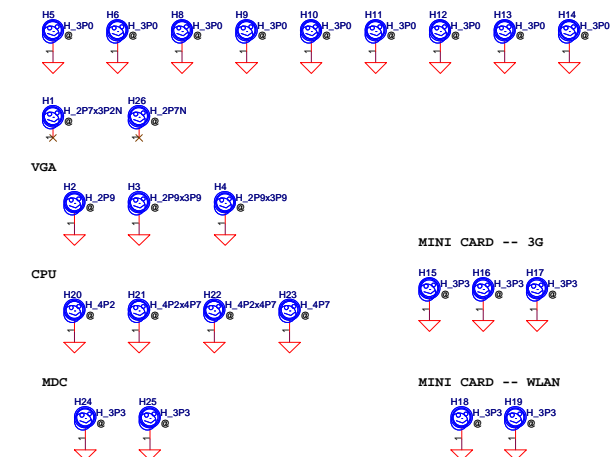
HDD LED



Logo LED



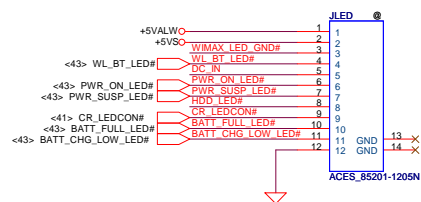
Screw Hole



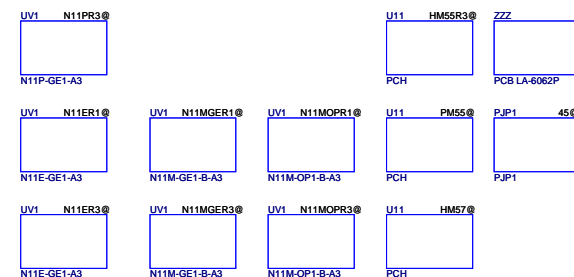
PCB Fedical Mark PAD



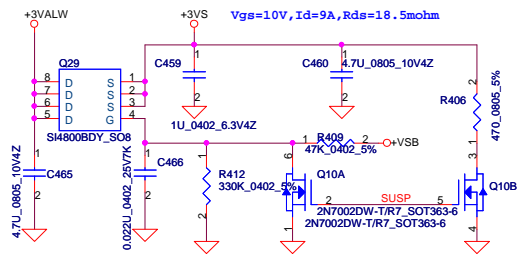
LED/B Connector



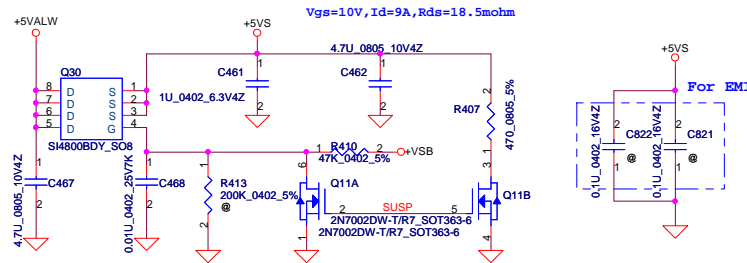
ISPD



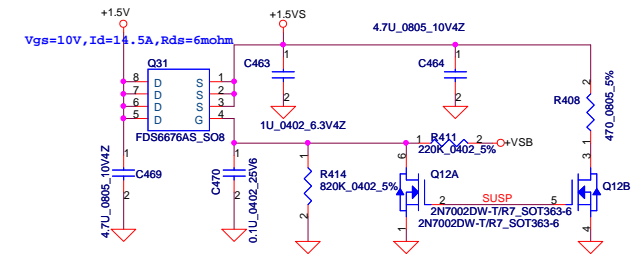
+3VALW TO +3VS



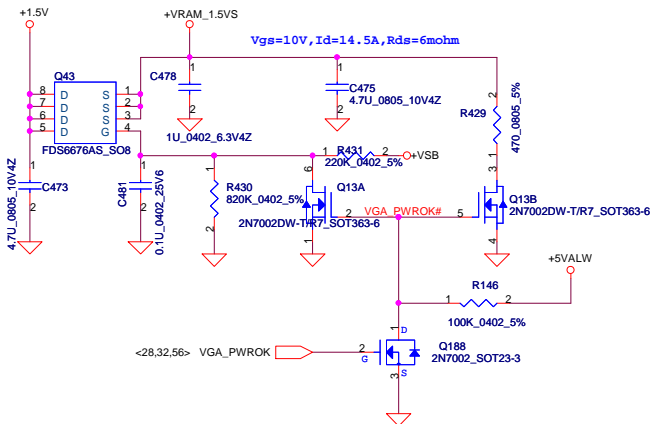
+5VALW TO +5VS



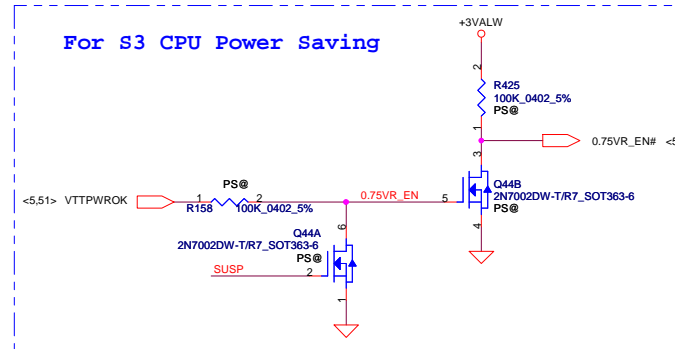
+1.5V to +1.5VS



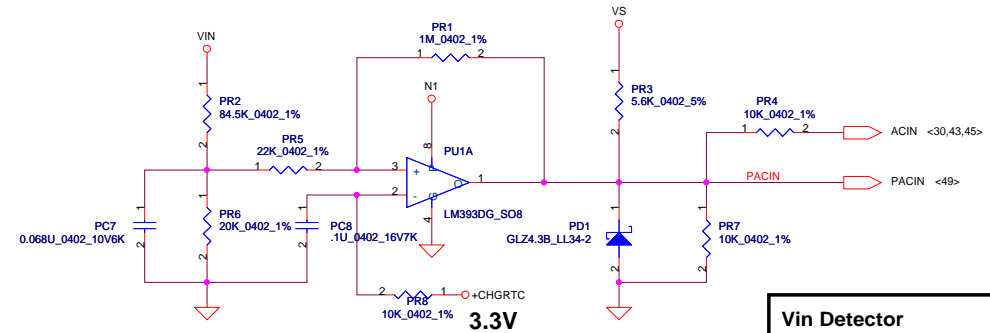
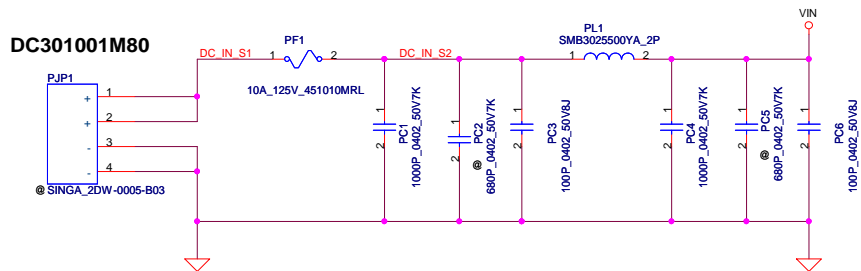
+1.5V to +VRAM_1.5VS



For S3 CPU Power Saving

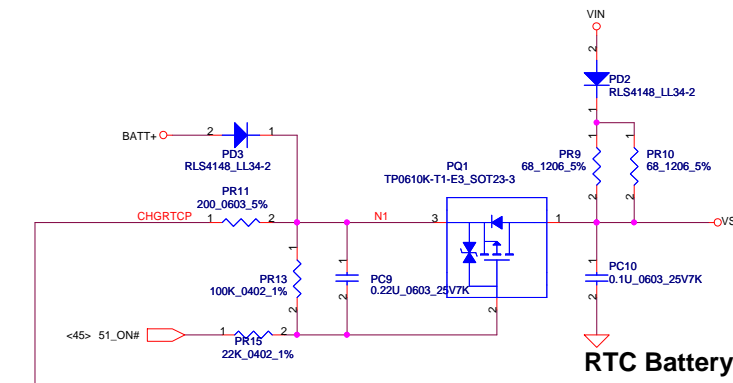


DC301001M80

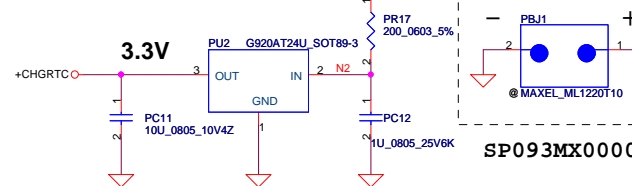


Vin Detector

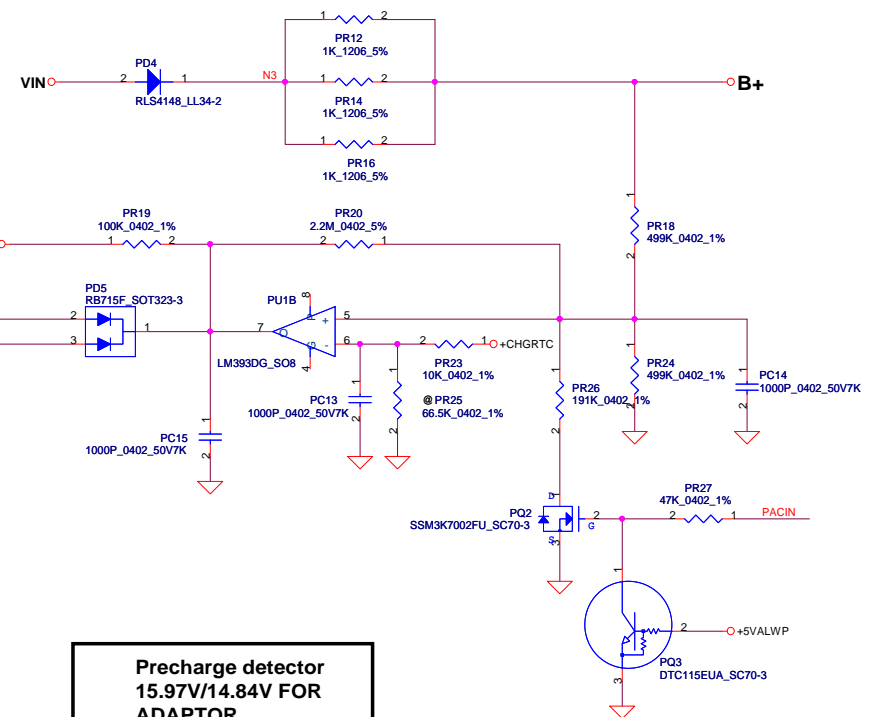
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



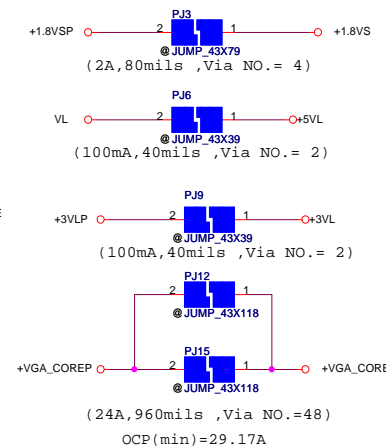
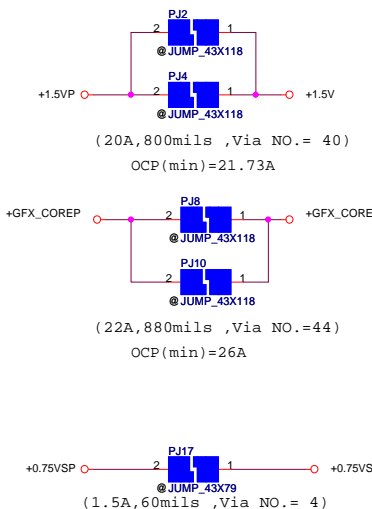
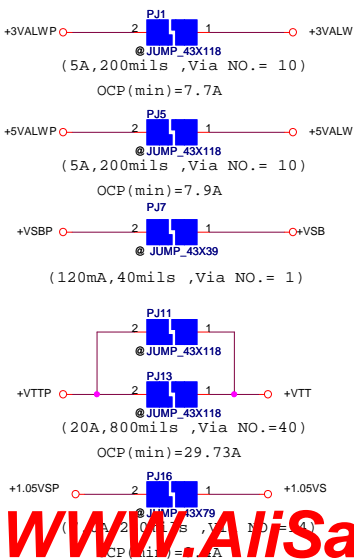
RTC Battery



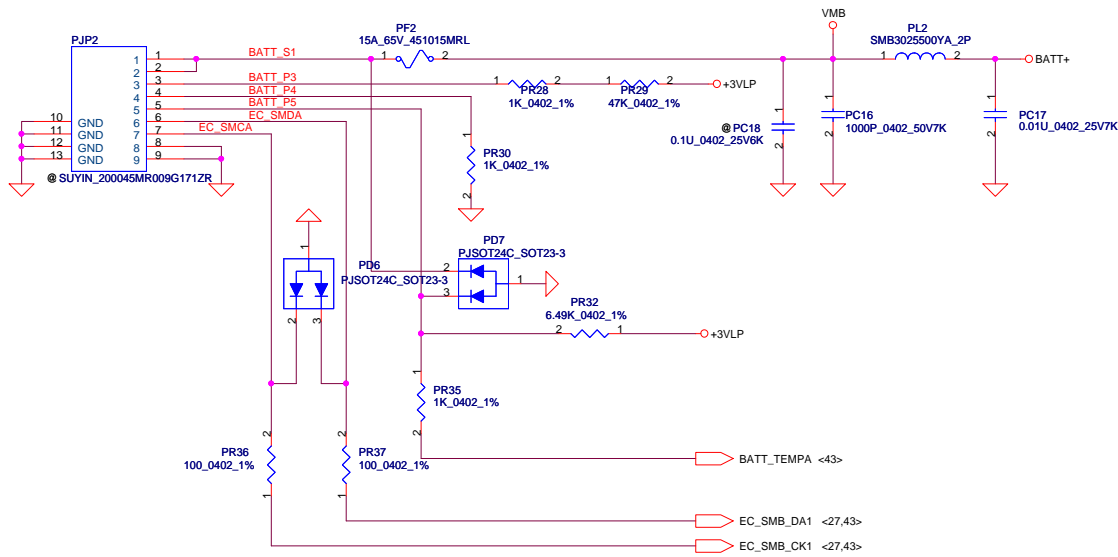
SP093MX0000



Precharge detector 15.97V/14.84V FOR ADAPTOR



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/01/23				DCIN / DETECTOR			
Deciphered Date				2010/01/23				NWQAA LA-6062P M/B			
Title				Size				Rev 2.0			
Document Number				Date				Wednesday, March 24, 2010			
Sheet				47				of 59			

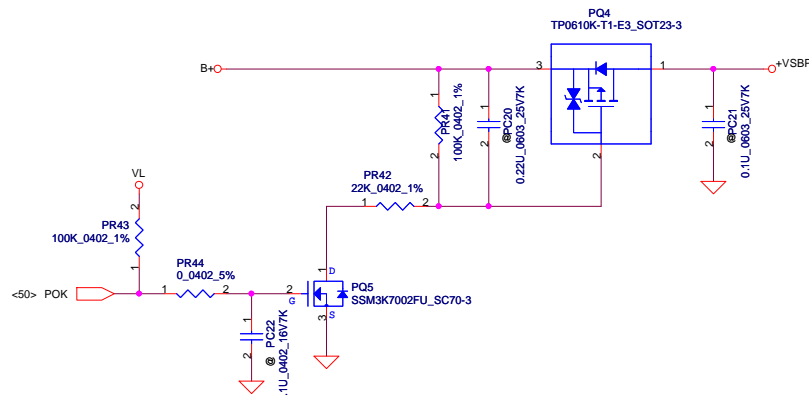
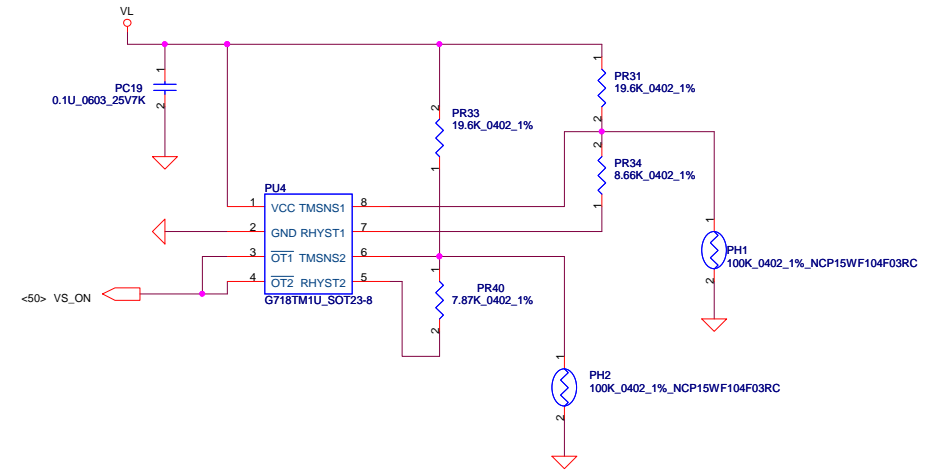


PH1 under CPU botten side :

CPU thermal protection at 95 degree C
Recovery at 56 degree C

PH2 near main Battery CONN :

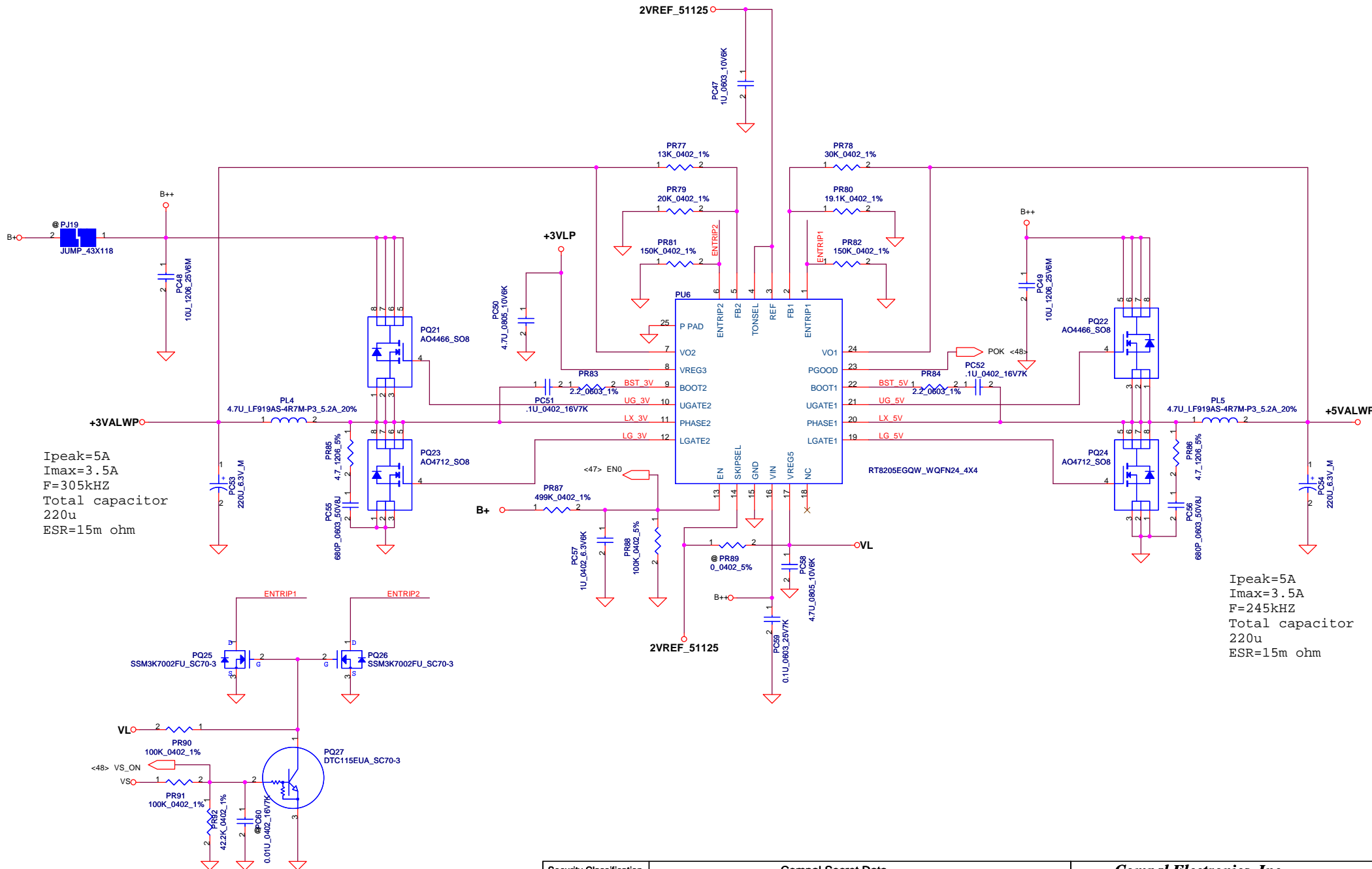
BAT. thermal protection at 95 degree C
Recovery at 48 degree C



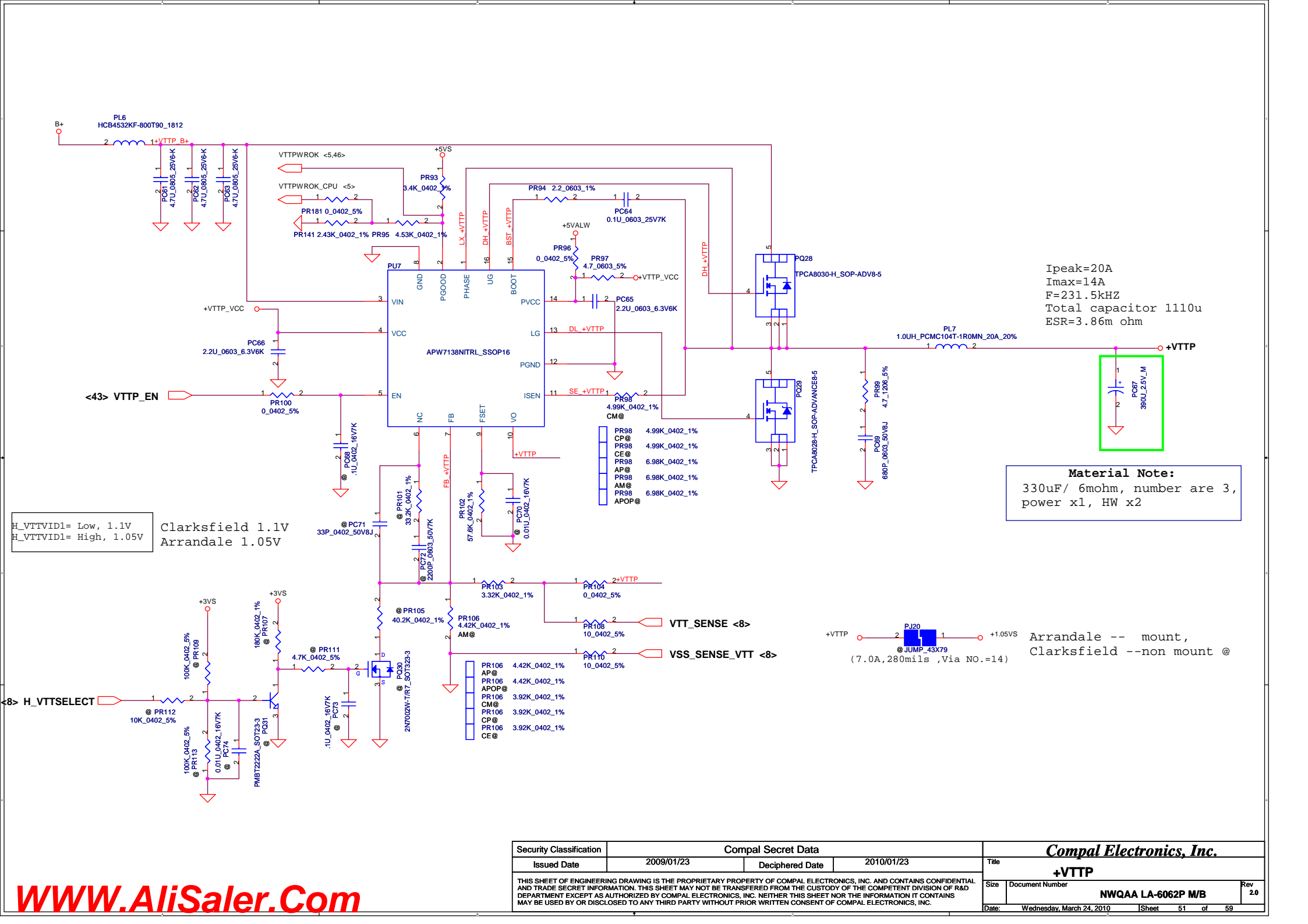
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
					NWQAA LA-6062P M/B
				Rev	2.0
				Date:	Wednesday, March 24, 2010
				Sheet	48 of 59



Date:	Wednesday March 24, 2010	Sheet	49	of	59
-------	--------------------------	-------	----	----	----



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				3VALWP/5VALWP	
Size	Document Number	Rev		2.0	
Date		Wednesday, March 24, 2010		Sheet 50 of 59	

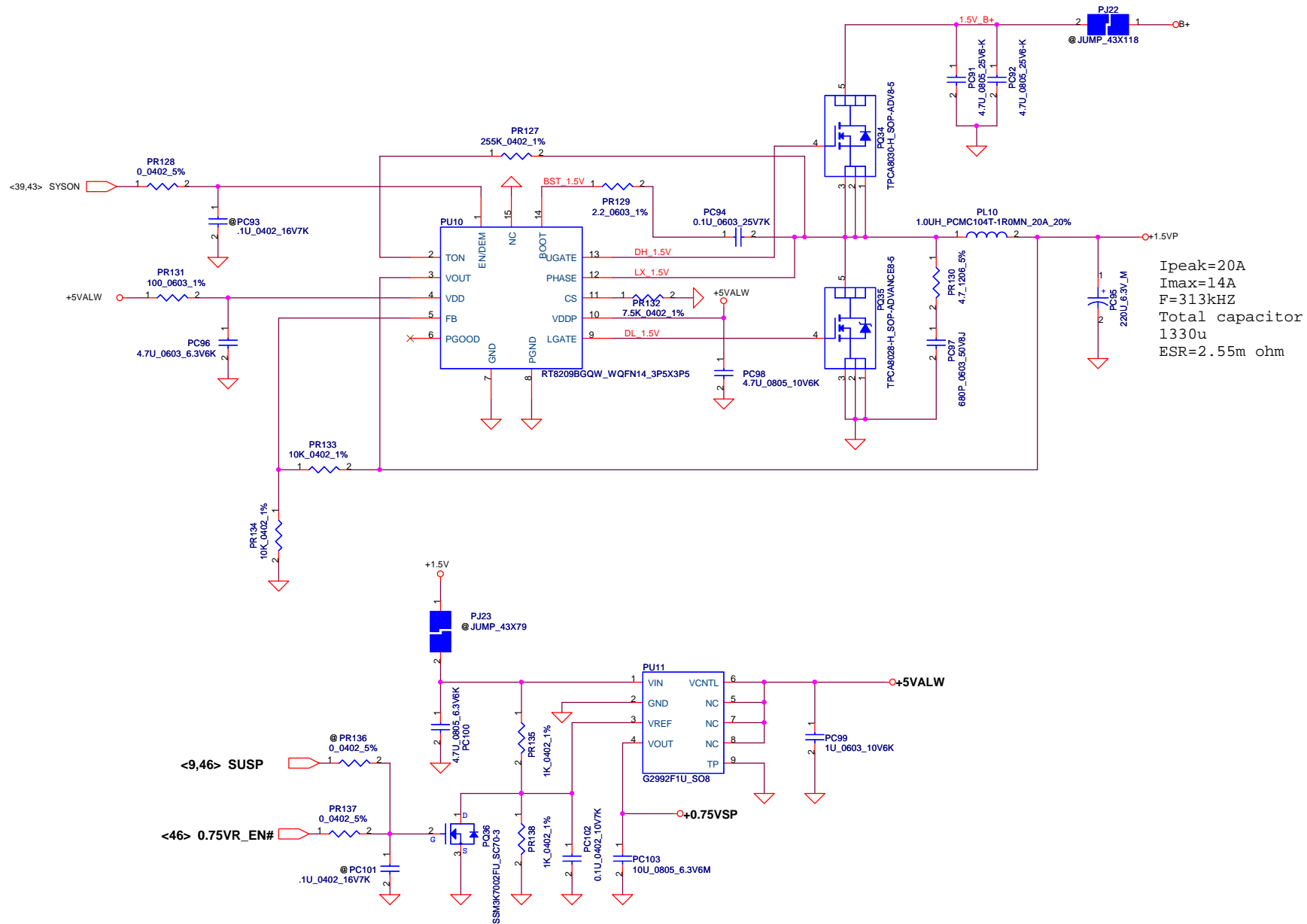


Ipeak=20A
Imax=14A
F=231.5kHz
Total capacitor 1110u
ESR=3.86m ohm

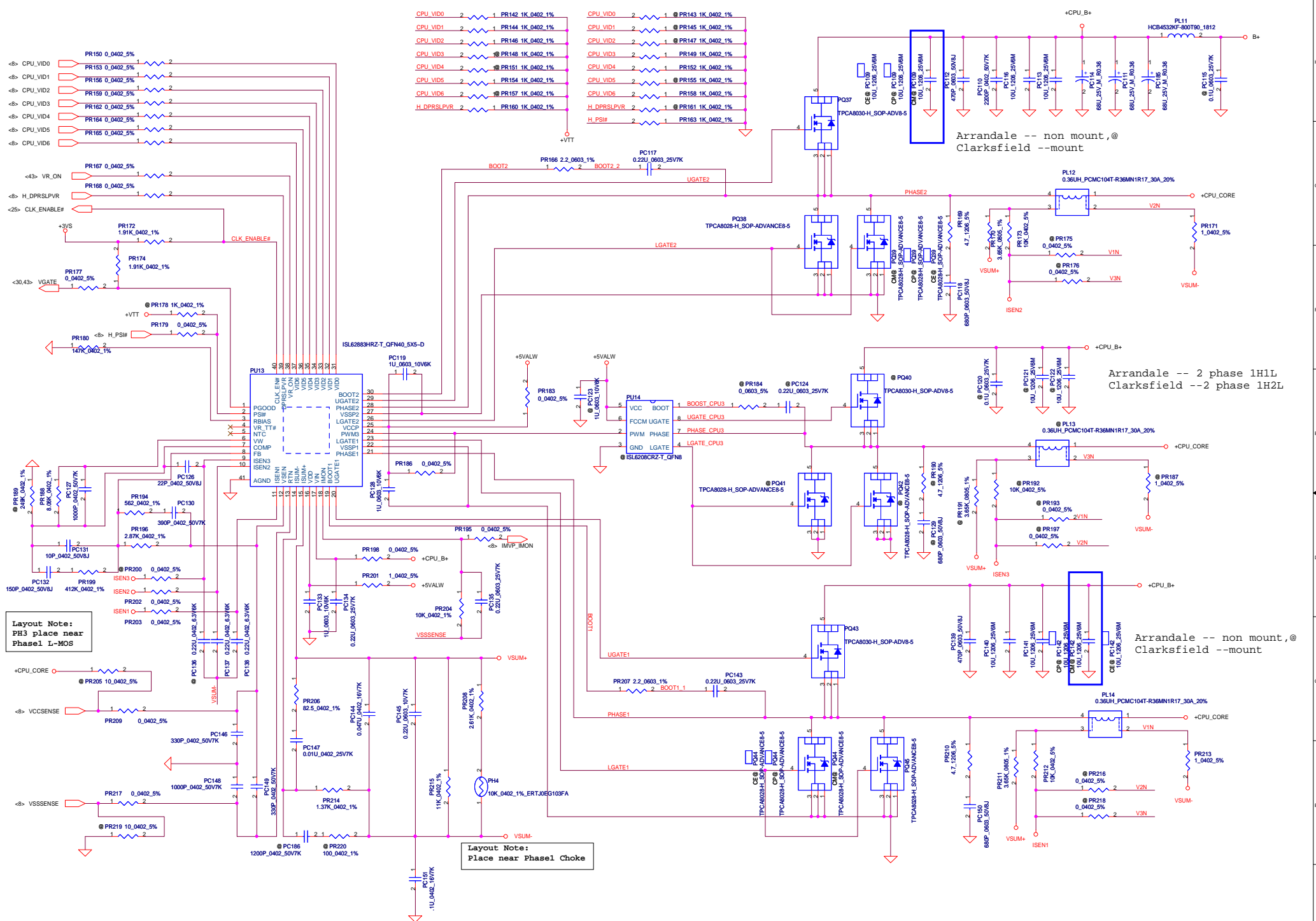
Material Note:
330uF/ 6mohm, number are 3,
power x1, HW x2

Arrandale -- mount,
Clarksfield --non mount @

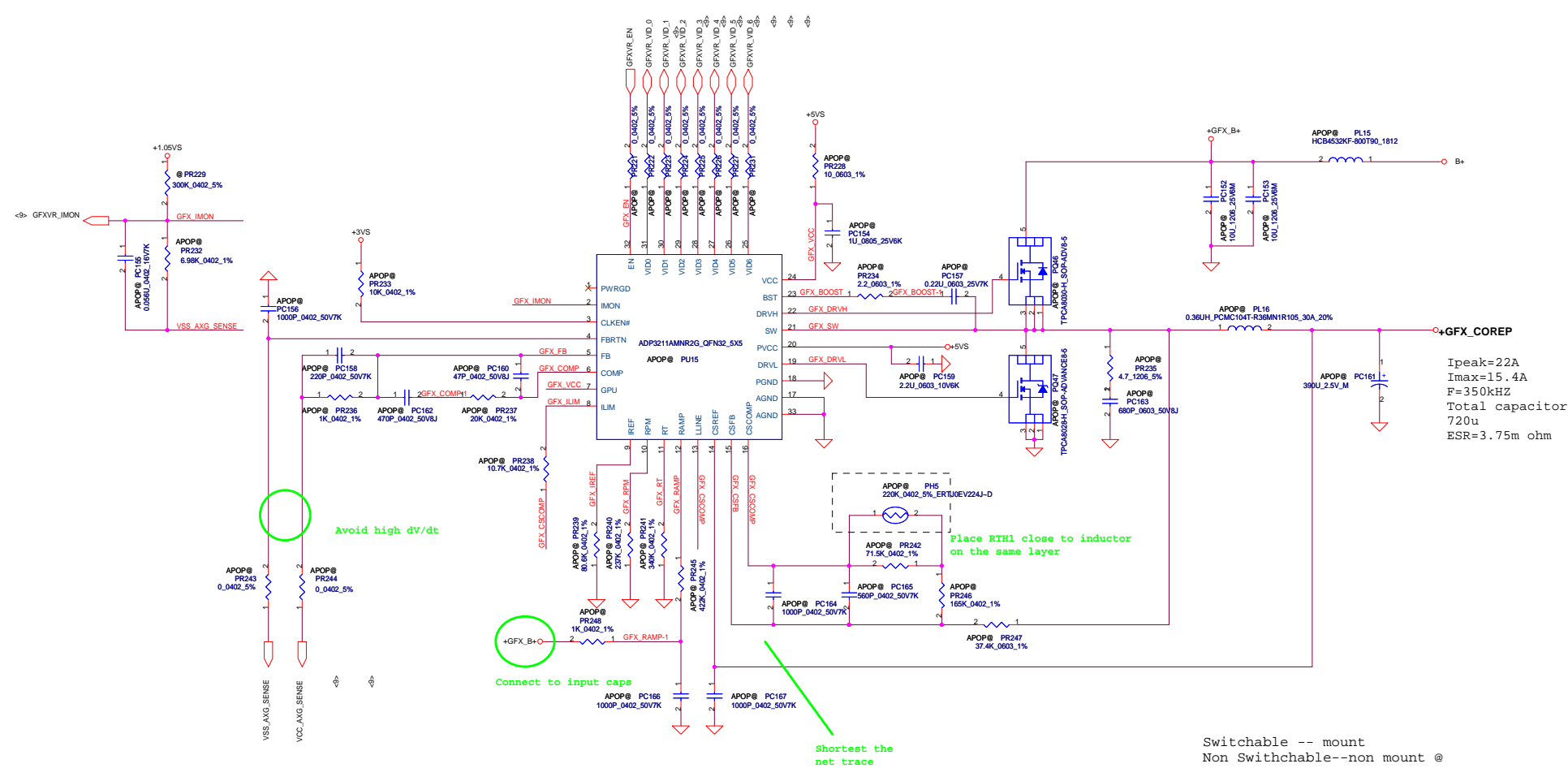
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2009/01/23		Deciphered Date		2010/01/23		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						+VTTTP					
						Size		Document Number		Rev	
								NWQAA LA-6062P M/B		2.0	
						Date: Wednesday, March 24, 2010		Sheet 51 of 59			



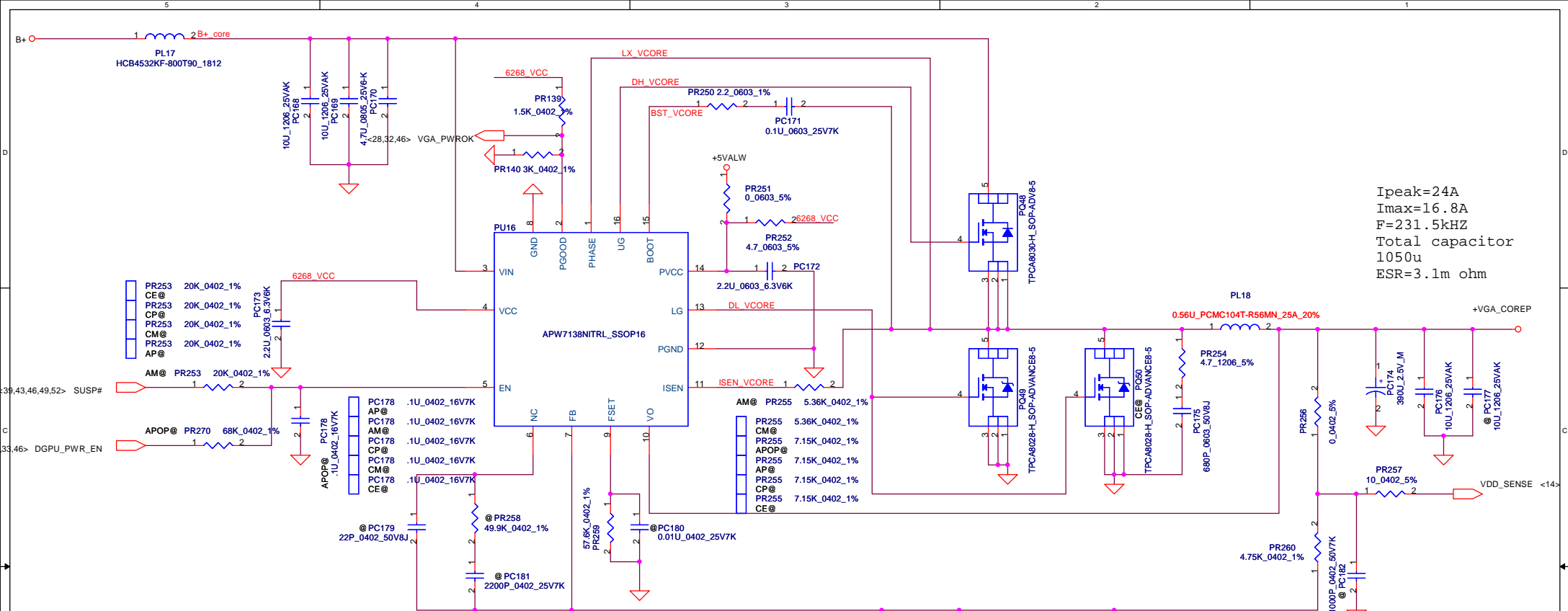
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title	+1.5VP/0.75VSP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	NWQAA LA-6062P M/B
				Date	Wednesday, March 24, 2010
				Sheet	53 of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				+CPU_CORE
Size	C	Document Number	NWQAA LA-6062P M/B	
Date	Wednesday, March 24, 2010	Sheet	54	of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/10/02	Deciphered Date	2010/10/02	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size
				Document Number
				Rev
				2.0
				Date: Wednesday, March 24, 2010
				Sheet 55 of 59



Ipeak=24A
Imax=16.8A
F=231.5kHz
Total capacitor
1050u
ESR=3.1m ohm

$$FSW = 1 / (75E-12 * 57.6K) = 231.48KHz$$

N11M-GE1/OP1	N11P-GE1	N11E-GE1_LP
Imax=16.09A Ipeak=18.19A Iocp=20.72A	Imax=16.8A Ipeak=24A Iocp=29.17A	Imax=16.8A Ipeak=24A Iocp=29.17A
PR255=5.36K PQ50=unpop	PR255=7.15K PQ50=unpop	PR255=7.15K PQ50=unpop

$$VFB(0.6) = Vout * Rbottom / (Rtop + Rbottom)$$

GPU_VID0	GPU_VID1	N11M-GE1/N11M-OP1	N11P-GE1	N11E-GE1_LP
0	0		0.80V	0.80V
1	0	0.85V	0.85V	0.85V
0	1			
1	1	1.03V	0.95V	0.9V
		PR260 = 4.75K PR262 = 14K PR261 = 56.2K PR263 = 16.2K	PR260 = 4.75K PR262 = 14K PR261 = 56.2K PR263 = 29.4K	PR260 = 4.75K PR262 = 14K PR261 = 56.2K PR263 = 63.4K

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/23	Deciphered Date	2010/01/23	+VGA_COREP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Rev 2.0
				Document Number	Document Number
				NWQAA LA-6062P M/B	
				Date: Wednesday, March 24, 2010	Sheet 56 of 59

NO DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT	P53-PWR_1.5VP/0.75VSP	Change PR132 18k to 6.19k	Modify 1.5V OCP to 18.09A (2009/11/25)
EVT	P56-PWR_VGA_COREP	Change PR270 0 to 100 Ohm	Adjust RC for Optimus sequence (2009/11/25)
		Change PC178 0.1U to 0.01U	
EVT	P39-PWR_+VTTP	Change PR141 2.26k to 2.43k	Modify VTTPWROK voltage (2009/11/25)
EVT	P39-PWR_+VTTP	Remove PC71 33P, PC72 2200P, PR101 33.2k	APW7138 not use this function (2009/11/25)
EVT	P38-PWR_3VALWP/5VALWP	Change PR92 49.9k to 42.2k	Modify VS divider voltage to drive MOS (2009/11/25)
EVT	P56-PWR_VGA_COREP	Remove PC179 22P, PC181 2200P, PR258 49.9k	APW7138 not use this function (2009/11/25)
EVT	P56-PWR_VGA_COREP	Change PR255 7.15k to 9.09k	Modify VGA 11P OCP to 38.03A (2009/11/25)
EVT	P56-PWR_VGA_COREP	Remove PC177 10U	FAE suggest to remove 1 10U cap for IC on time control (2009/11/25)
EVT	P42-PWR_CPU_CORE	Change PL12,PL14 SH000005680 to SH00000IK00	Use 5% DCR choke (2009/11/25)
EVT	P43-PWR_GM VGA_CORE	Change PH5 SL20000058L to SL2000000500	Use Compal PN (2009/11/25)
DVT	P56-PWR_VGA_COREP	Change PR255 9.09k to 7.15k	Modify VGA 11P OCP to 29.17A (2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change PL16 SH00000HK00 to SH00000IK00	Use same PN choke (2009/12/28)
DVT	P39-PWR_+VTTP	Change PR106 4.42k to 3.92k	Modify VTT voltage to 1.1V for Clarkfield (2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PC114, PC111, PC185 from SF000000F80 to SF000000W00	Cost down (2009/12/28)
DVT	P43-PWR_GM VGA_CORE	Change PC161 to SGA00002680	For DVT budding(thermal issue), it will change to original type for PVT (2009/12/28)
DVT	P56-PWR_VGA_COREP	Change PR253 0 to 20k	For VGA sequence(2009/12/28)
DVT	P56-PWR_VGA_COREP	Change PR270 0 to 20k	For VGA sequence(2009/12/28)
DVT	P52-PWR_1.05VSP/1.8VSP	Add PC83 0.1U and change PR122 0 to 68k	For VGA sequence(2009/12/28)
DVT	P48-PWR_BATTERY CONN / OTP	Add PD6, PD7 ESD diode	For ESD solution(2009/12/28)
DVT	P49-PWR_CHARGER	Add PC104,PC105,PC106 10U	Reserve for EMI solution(2009/12/28)
DVT	P50-PWR_3VALWP/5VALWP	Change PR83,PR84 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR85,PR86 4.7 and PC55,PC56 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P42-PWR_CPU_CORE	Change PR166,PR207 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR169,PR210 4.7 and PC118,PC150 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P55-PWR_GM VGA_CORE	Change PR234 0 to 2.2	Add boost resistor(For EMI solution)(2009/12/28)
		Add PR235 4.7 and PC163 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P56-PWR_VGA_COREP	Add PR254 4.7 and PC175 680P	Add snubber(For EMI solution)(2009/12/28)
DVT	P48-PWR_BATTERY CONN / OTP	Change PR33 10k,PR31 21k to 19.6k, PR34 9.53k to 8.66k, PR40 47k to 7.87k	Adjust OTP setting point(2009/12/28)
DVT	P42-PWR_CPU_CORE	Add PQ39,PQ44 TPCA8028-H	Use 1H 2L MOS solution for Clarksfield (2009/12/31)
DVT	P42-PWR_CPU_CORE	Add PC109,PC142 10U input cap	For Clarksfield solution (2009/12/31)
DVT	P42-PWR_CPU_CORE	Change PR214 1.2k to 1.37k	Adjust CPO_CORE OCP to 65A (2009/12/31)
DVT	P42-PWR_CPU_CORE	Change PR196 2.43k to 2.87k	Adjust CPU_CORE load line (2009/12/31)
DVT	P42-PWR_CPU_CORE	Change PR204 8.25k to 10k	Adjust resistor for Imon (2009/12/31)
DVT	P39-PWR_+VTTP	Change PR98 4.99k to 6.98k	Adjust VTT_DIS_Arrandale OCP to 29.73A (2009/12/31)
DVT	P53-PWR_1.5VP/0.75VSP	Change PR132 6.19k to 7.5k	Adjust 1.5V OCP to 21.73A(2009/12/31)
DVT	P52-PWR_1.05VSP/1.8VSP	Change PQ33 from FDS6670 to AO4712	Change design rating(2009/12/31)
DVT	P39-PWR_+VTTP	Change PR98 6.98k to 4.99k	Adjust VTT_DIS_Clarksfield OCP to 20.64A (2009/12/31)
DVT	P55-PWR_GM VGA_CORE	Change PR247 34.8k to 37.4k	Adjust GFX load line (2009/12/31)
DVT	P41-PWR_0.75VSP/1.8VSP	Change PC90 SE025681K80 to SE024681J80	Use same PN (2009/12/31)
DVT	P56-PWR_VGA_COREP	Change PR270 20k to 68k, PC178 0.01U to 0.1U	Adjust Optimus sequence (2010/01/06)
PVT	P41-PWR_0.75VSP/1.8VSP	Remove PR136, Add PR137 0 Ohm	For S3 power saving function (2010/02/03)
PVT	P43-PWR_GM VGA_CORE	Change PC161 to SF000002000	Change to original type for PVT (2010/02/03)
PVT	P49-PWR_CHARGER	Change PC24,PC25,PC26 4.7U to 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC107 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P49-PWR_CHARGER	Add PC104,PC105,PC106 10U	For EMI solution(ISN test) (2010/02/03)
PVT	P38-PWR_3VALWP/5VALWP	Change PQ27 from SSMK7002 to DTC115EUA	Use low Vth Transistor (2010/02/03)
PVT	P52-PWR_1.05VSP/1.8VSP	Change PR119 10k to 15.8k	Adjust 1.05V OCP to 8.47A (2010/02/03)

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2009/01/23	Deciphered Date	2010/01/23	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Power PIR		
				Size	Document Number	Rev
					Calpella common	2.0
Date: Tuesday, March 23, 2010		Sheet		57	of	59

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
Pre MP		P52-PWR_1.05VSP/1.8VSP	Change PR123 316k to 25.5k,PR124 402k to 51.1k	Adjust 1.8V voltage divided resistor (2010/03/07)
Pre MP		P52-PWR_1.05VSP/1.8VSP	Change PU9 from MP2121 to SY8033	MP2121 ESD fail (2010/03/07)
Pre MP		P52-PWR_1.05VSP/1.8VSP	Delete PR125 0 Ohm	Change for SY8033 solution(2010/03/07)
			Change PC85 from 0.1U to 22U	
			Delete PC87 10UF, PC84 0.1U	
Pre MP		P52-PWR_1.05VSP/1.8VSP	Change PC86 10U to 68P	Improve 1.8V transient under shoot(2010/03/07)
Pre MP		P49-PWR_CHARGER	Change PC24,PC25,PC26 10U to 4.7U	10U 0805 size price too high(2010/03/07)
Pre MP		P47-PWR_DCIN/DECTOR	Change PC12 from SE033105Z80 to SE000001380	Change PN(2010/03/07)
Pre MP		P49-PWR_CHARGER	Change PR68 from 53.6k to 24k, PR45 from 0.015 to 0.02 Ohm	Change CP from 90W to 75W(For cost down)(2010/03/07)
Pre MP		P49-PWR_CHARGER	Change PQ6,PQ7 from AO4407A to AO4435	Change MOS reting for 75W adapter(For cost down)(2010/03/07)
Pre MP		P56-PWR_VGA_COREP	Add PR264,PR267 100k	Use 100k resistor to pull high +3VS_DGPU(Set initial VID to P0 state)(2010/03/07)

Security Classification		Compal Secret Data		Title	
Issued Date		2009/01/23	Deciphered Date	2010/01/23	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size			Rev
		Document Number			2.0
Date:		Tuesday, March 23, 2010		Sheet	58 of 59

HW PIR (Product Improve Record)

NWQAA LA-6062P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1 TO 0.2

GERBER-OUT DATE: 2009/12/30

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	12/7	37	Add +5VALW and +5VL for JPIO pin5	For BACK_SENSE detect
2	12/7	46	Change PJ32 to R104 and PJ33 to R144	For discrete BOM structure
3	12/7	25	Remove JLVDS pin10 and pin12 for +LCDVDD_R	3D Panel max. current is 1.5A
4	12/8	45	Combine JTOUCH and JLP to JTPL and remove C648	For ME cost down
5	12/8	13	Add QV2, RV110, RV123 and RV124	For CLK_REQ_VGA# level shifter
6	12/14	25	Add C495 and C496	For RF request
7	12/15	33	Add R258	For OPTIMUS_EN#
8	12/15	34	Add C499	For power team request
9	12/17	45	Remove D19	Move D19 to LS-6061P
10	12/18	38	Reverse JBT pin definition	Due to pin reverse
11	12/18	42	Add RA42	For codec EC_MUTE# issue
12	12/21	41	Change JREAD to Push-push type (R015-211-1M-A)	For PRD update
13	12/21	25	Move LED_PWM and BKOFF#_R to JLVDS pin10 and pin12	For avoiding +LCD_INV short issue
14	12/22	44	Change H7 footprint to "DEBUG_PAD-MB-S"	For debug use
15	12/23	39	Add D24 and Q36 for BT_CTRL	For WLAN & BT combo module
16	12/23	33	Add R461	For CIR_EN#
17	12/24	25	Mount C236 and C268	For ESD request
18	12/24	37	Change JPIO footprint and reverse its pin definition	For ME request
19	12/24	27	Add R145	For U9 ESD damage issue
20	12/24	41	Add F3	For connector short issue
21	12/28	42	Change RA41 to SM01000CY00 (FBMA-10-100505-301T)	For EMI request
22	12/28	25	Remove L1	For 3D panel
23	12/29	42	Change RA1, RA18 and RA20 to SM01000B200	For RF request
24	12/29	25	Change C484 to 100P	For RF request
25	1/6	37	Change C426 to SF0000001500	For cost down
26	1/12	38	Change R132 BOM from FLICA@ to FELICA@	For Felica issue
27	1/12	11	Change C218 to SF0000002000	For cost down
28	1/12	8	Change C144 to SF0000002200	For thermal interfere issue

NWQAA LA-6062P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.2 TO 0.3

GERBER-OUT DATE: 2010/02/08

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	1/15	42	Add RA43	For sleep & music on battery mode
2	1/15	46	Change +1.05VS_DGPU to N-MOS	For +1.05VS_DGPU drop issue
3	1/21	43	Add R462	Avoid VR_ON floating
4	1/25	44	Change UG3 to SA000022I00	For LDO issue
5	1/25	45	Change SW2 to @	For ME interfere issue
6	1/27	9	Change CV57, CV58 abd C271 to OS-CON	For cost down
7	2/1	25	Add +LCD_VDD to JLVDS pin18	For CMO 3D Panel
8	2/1	27	Add R208	For AOC monitor issue
9	2/1	43	Change U19 to SA00001J5A0	For KB926 E0 version
10	2/1	39	Add +1.5VS for J3G	For TV tuner MC770A
11	2/1	41	Remove F3	For UC1 ES2 sample
12	2/2	43	Add CAP_RST# to EC	For ESD issue
13	2/3	41	Change RC7 to 33 ohm	For EMI request
14	2/4	42	Remove RA40, add RA44 and RA22	For audio issue
15	2/4	14	Reserve VBIOS ROM	For SW request
16	2/5	32	Swap USB port4 and port8	For customer request
17	2/5	13	Reserve 27MHz crystal	For HDMI issue
18	2/9	40	Change L11 to 2.2U and C113 to 4.7U	For Realtek request
19	2/10	41	Change RC7-RC14 to 22 ohm	For O2 request
20	2/10	27	Remove HDMI common mode choke	For cost down

NWQAA LA-6062P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.3 TO 1.0

GERBER-OUT DATE: 2010/03/15

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/6	32	Change R390 to 1K	For Optimus sequence
2	3/6	33	Change R59 to 1K	For Optimus sequence
3	3/6	27	Change Q18 and Q19 power to +3VS_DGPU	For GPU power rail
4	3/6	41	Add QC2 and RC16	For O2 B0 workaround
5	3/7	28	Change D13.2 power to +CHGRTC	For RTC issue
6	3/8	32	Add R333 and R334	For Optimus sequence
7	3/8	25	Add BOM structure 3D@ and NO3D@	For 3D SKU PWM
8	3/8	13	Change YV1 to SJ100006R00	For cost down
9	3/11	46	Change C685 to 0603 size	For ME height limit
10	3/11	45	Change H15-H19 to H_3P3	For ME request
11	3/15	45	Remove SW2	For ESD request
12	3/15	42	Change CA9 and CA10 to 1U	For cut-off frequency
13	3/16	42	Change MONO_IN to AGND	For high frequency noise issue

NWQAA LA-6062P SCHEMATIC CHANGE LIST

REVISION CHANGE: 1.0 TO 2.0

GERBER-OUT DATE: 2010/03/19

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/17	41	Change cardreader to JMB385/389	For customer request
2	3/18	34	Add R49	For CRT wave issue
3	3/19	13	Change LV3 to always stuff	For NVIDIA request
4	3/19	34	Change L12 to 2.2 ohm for Optimus SKU	For CRT wave issue
5	3/22	27	Add D54	For HDMI CEC issue
6	3/24	25	Chane C214 to 1U	For NALAA ESATA performance low issue

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	200910/9	Deciphered Date	2010/01/23	Title	HW-PIR
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc. Number	NWQAA LA-6062P M/B
Date:	Wednesday, March 24, 2010	Sheet	59	of	59